

# Hadley15'' Schematics Document

## Haswell ULT

**2013-06-28**  
**REV : A00**

*DY : None Installed*  
*UMA: UMA only installed*  
*OPS: Optimus solution installed.*  
*eDP: Support eDP Panel installed.*  
*LVDS: Support LVDS Panel installed.*

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Title

**Cover Page**

Size  
A3

Document Number

**Hadley 15''**

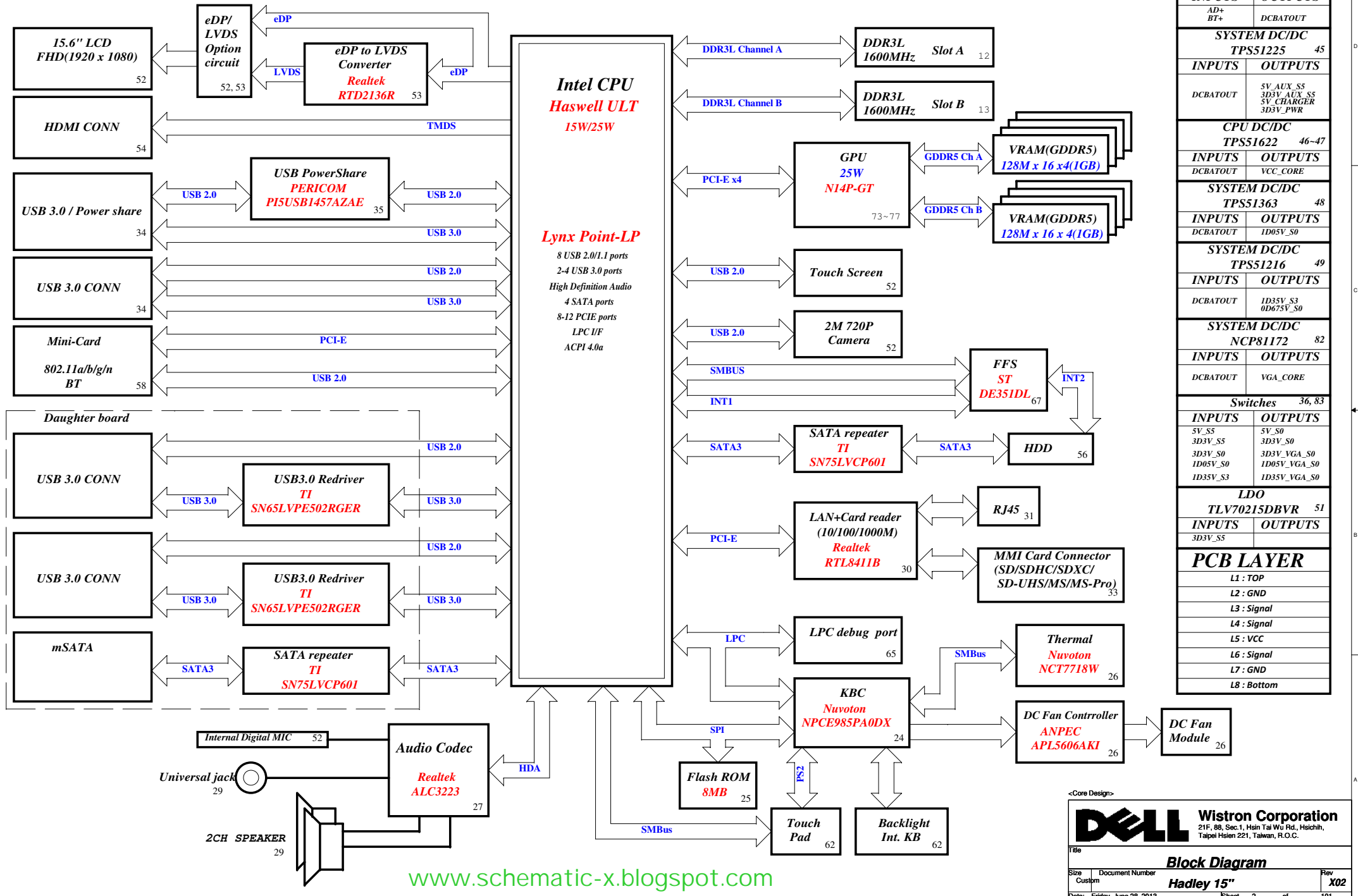
Rev  
**X02**

Date: Friday, June 28, 2013

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# Hadly15 Block Diagram

Project code : 91.47L01.001  
PCB P/N : 12311-1  
Revision : A00



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SSID = CPU<sup>5</sup>



Impedance control:50 ohm



Design Guideline:  
SM\_RCOMP keep routing length less than 500 mils.



Place close to DIMM

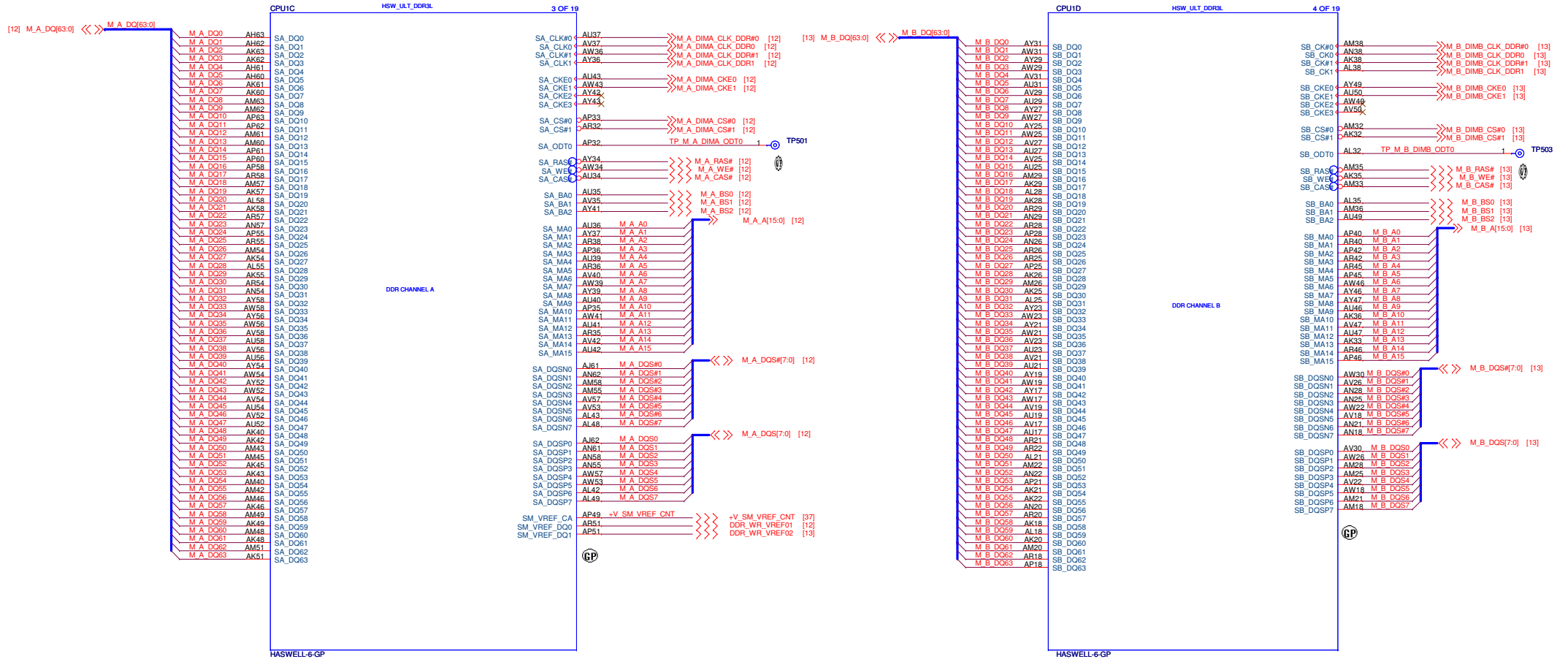
**CPU (THERMAL/CLOCK)**

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# SSID = CPU

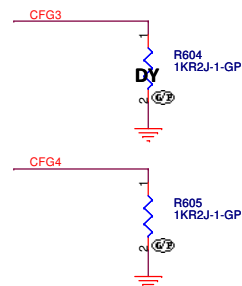
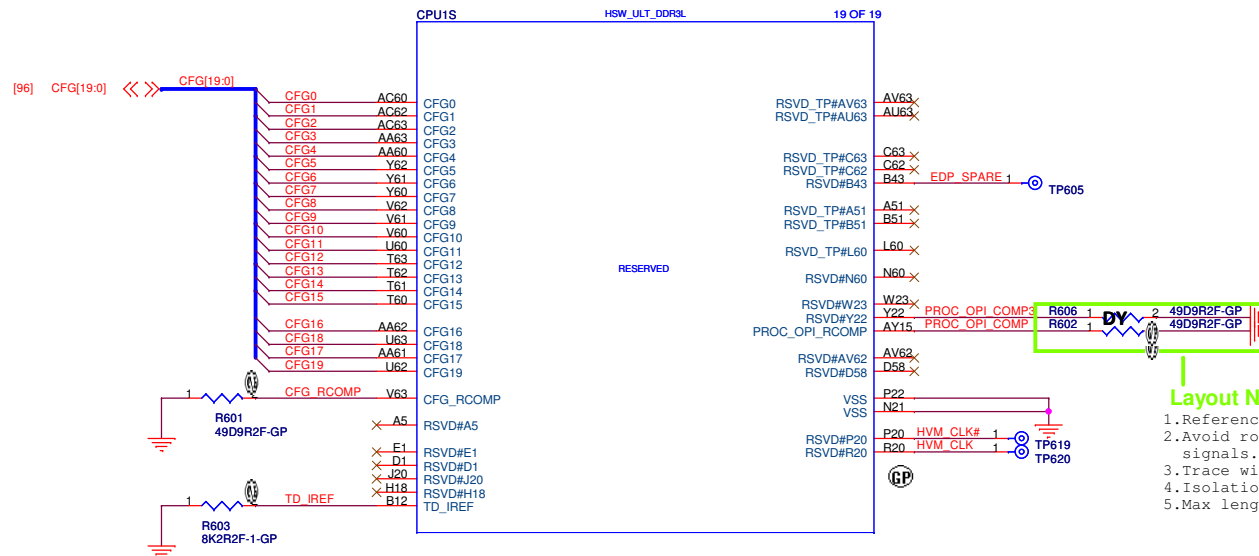


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Title		CPU (DDR)	
Size	Custom	Document Number	Hadley 15"
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SSID = CPU



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

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**CPU (RESERVED)**

Size  
A3

Document Number

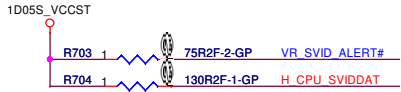
**Hadley 15"**

Rev  
**X02**

Date: Friday, June 28, 2013

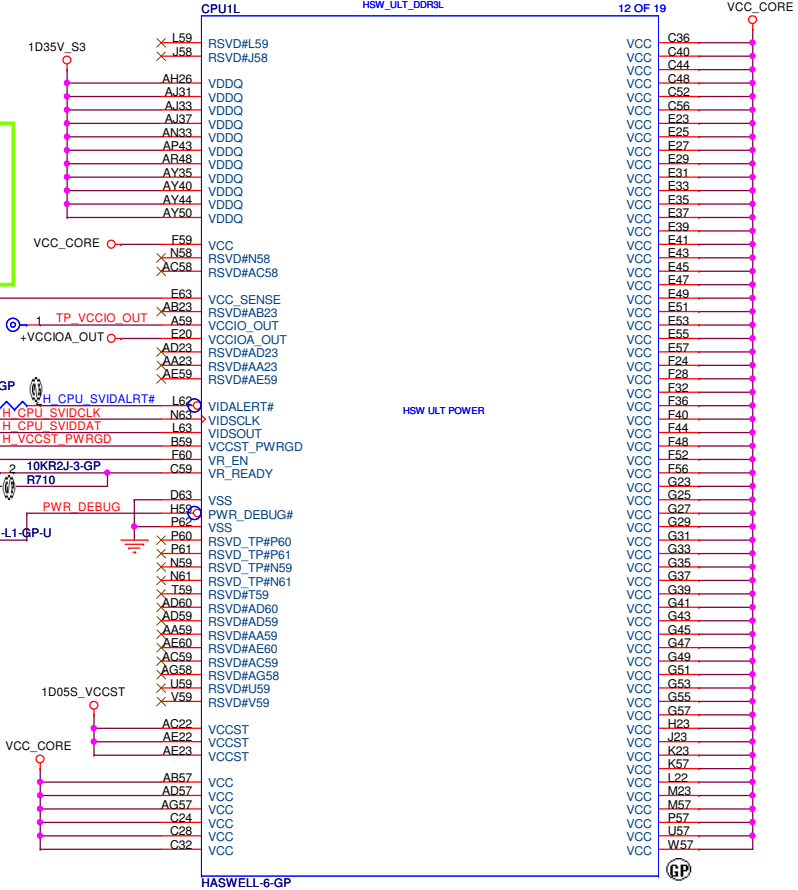
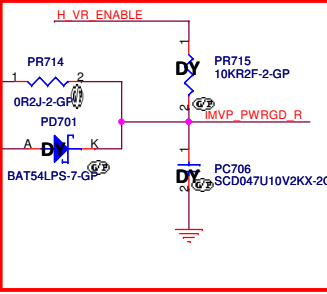
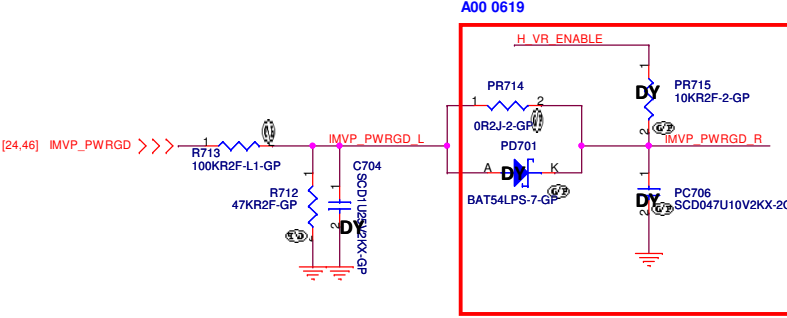
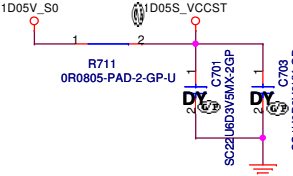
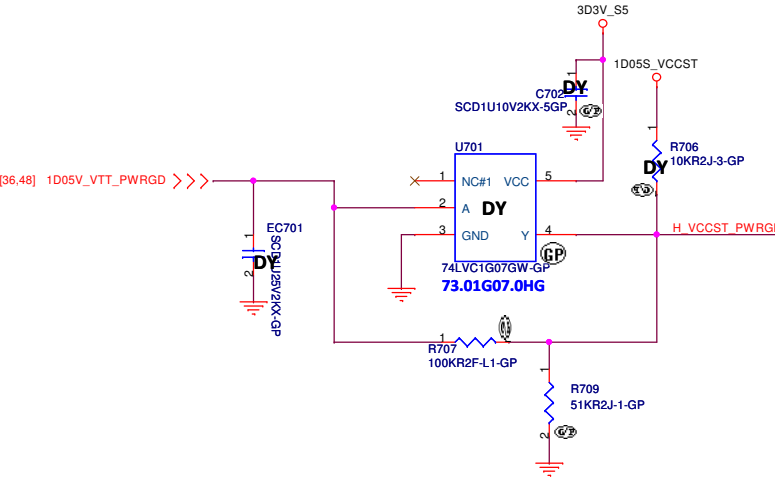
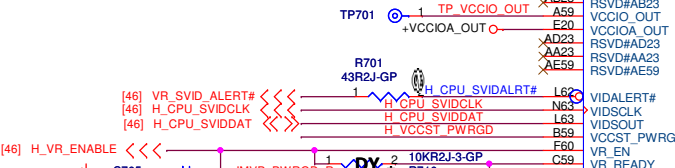
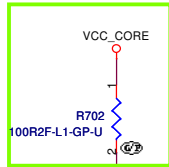
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**SSID = CPU**



**Layout Note:**

1. Place close to CPU
2. VCC\_SENSE/ VSS\_SENSE  
impedance=50 ohm
3. Lwngth match<25mil



## Core Design



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**CPU (VCC CORE)**Size  
A3

Document Number

### ***Hadley 15"***

X02

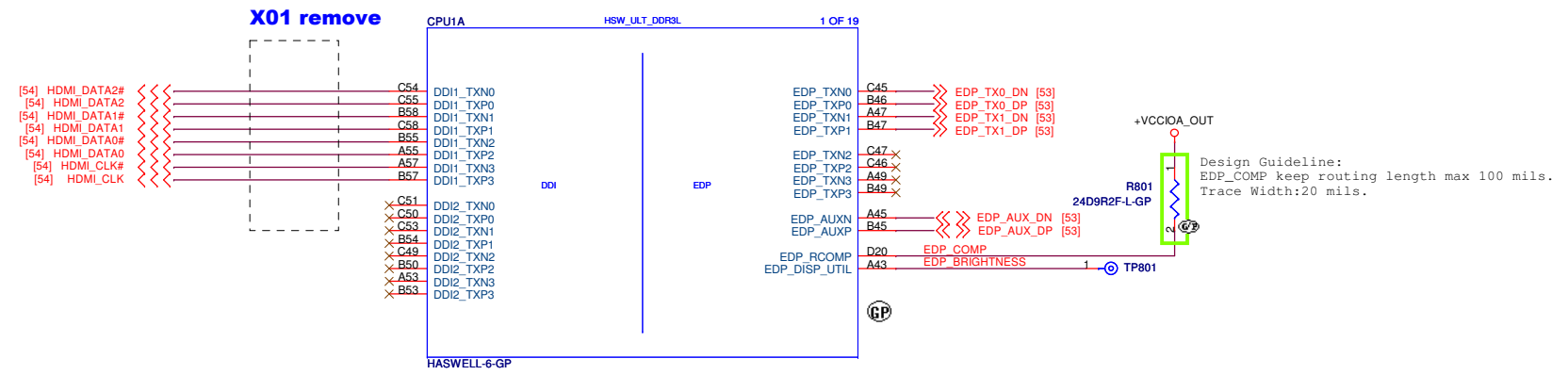
Date: Friday, June 28, 2013

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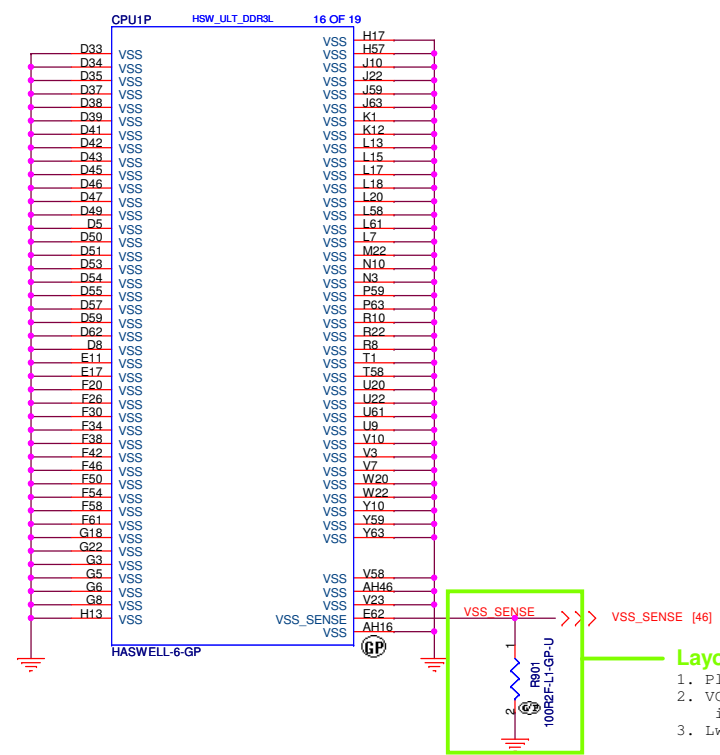
SSID = CPU

HDMI



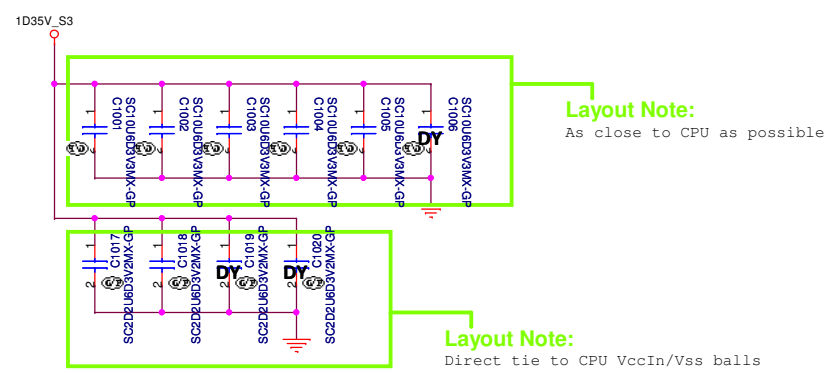


SSID = CPU

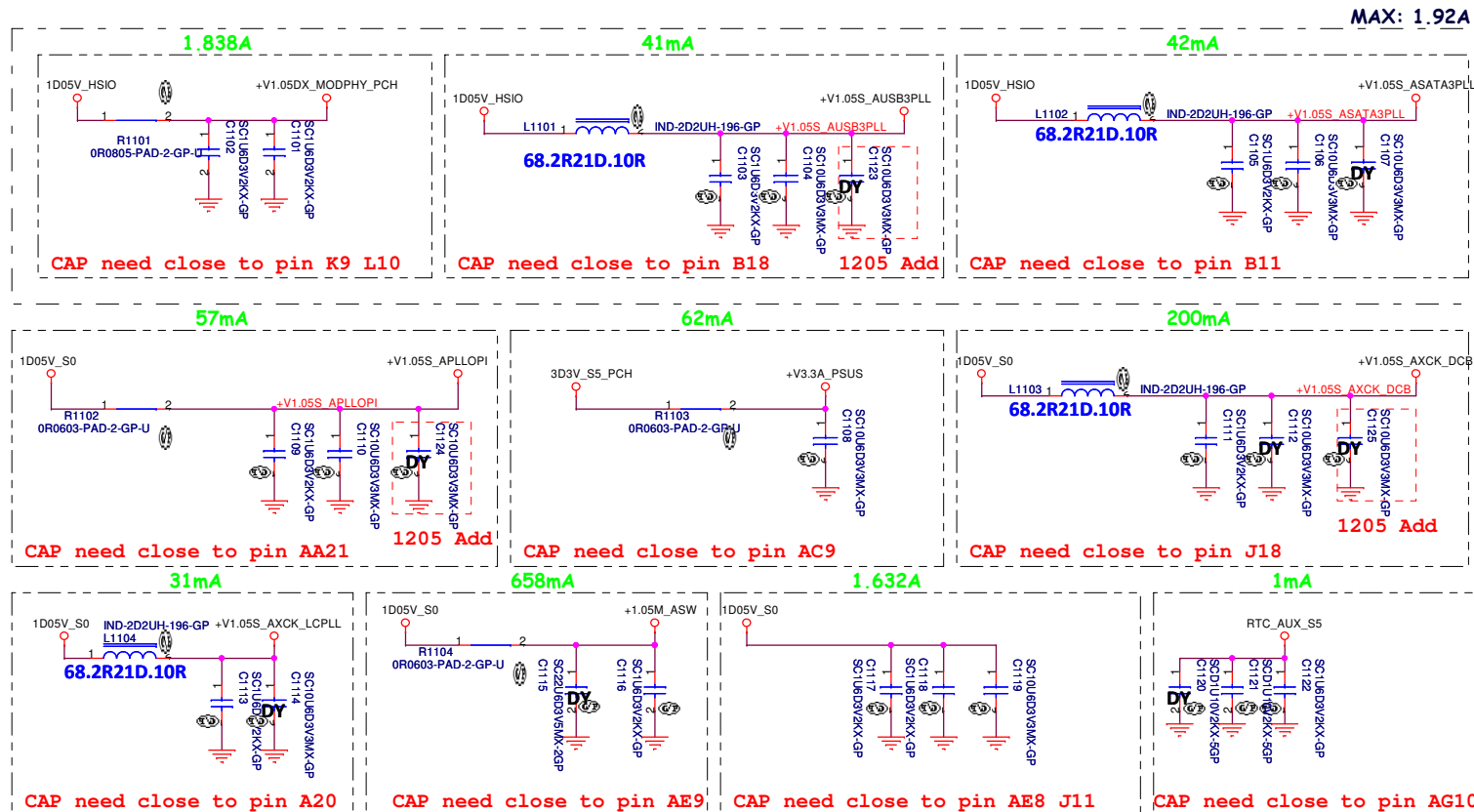


- Layout Note:**
1. Place close to CPU
  2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
  3. Lwnngth match<25mil

SSID = CPU



SSID = CPU



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**CPU(Power CAP2)**

Size

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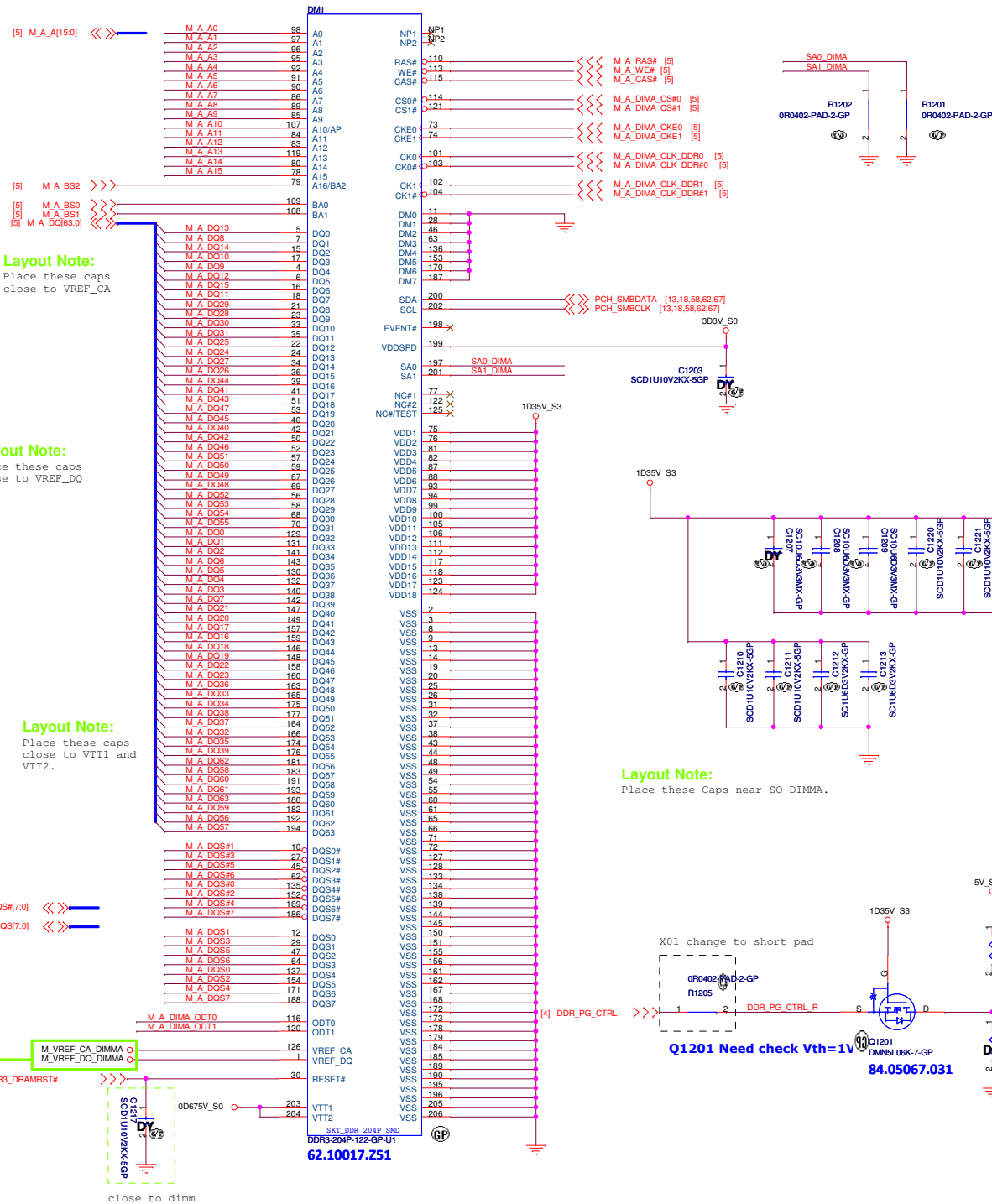
Rev

**X02**

Date: Friday, June 28, 2013

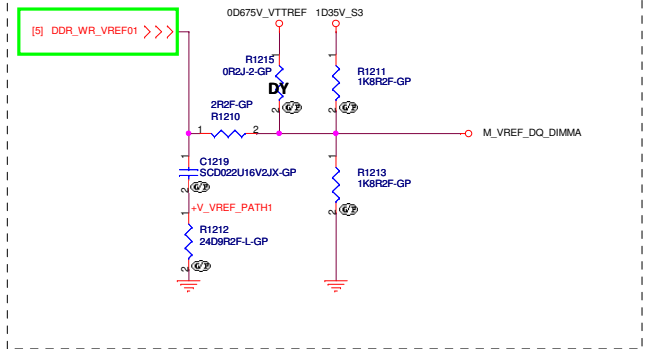
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## SSID = MEMORY

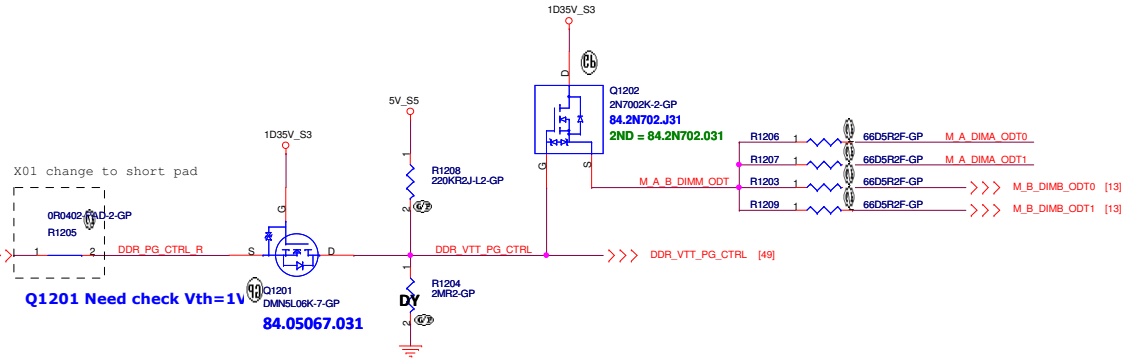


**Note:**  
SA0 DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SQ-DIMMA TS Address is 0x30

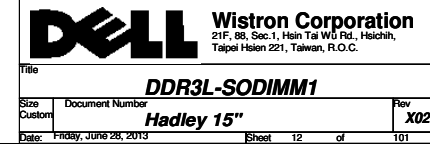
**Layout Note:**  
Place Close SO-DIMMA.



**Layout Note:**  
Place these Caps near SO-DIMM.




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Size  
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Document Number

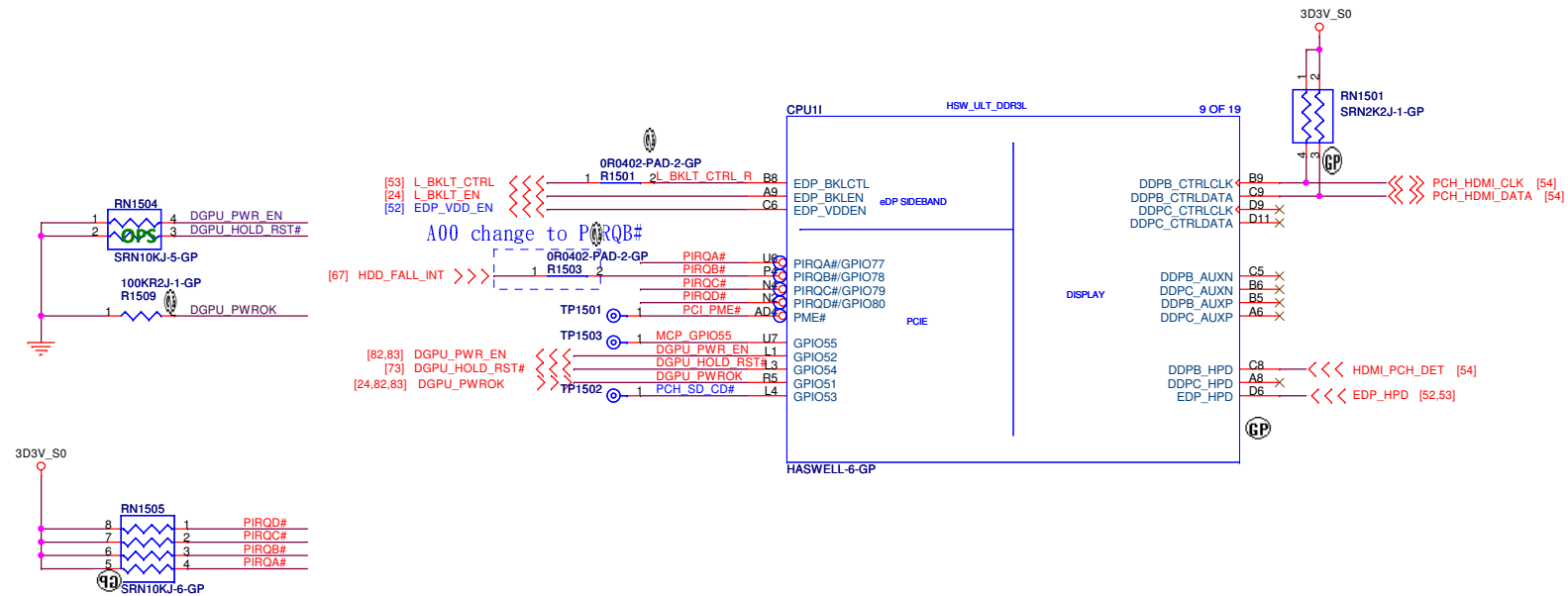
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X02

Hadley 15"

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**SSID = CPU**



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**CPU ( EDP SIDEBAND/GPIO/DDI )**

Size

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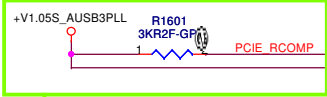
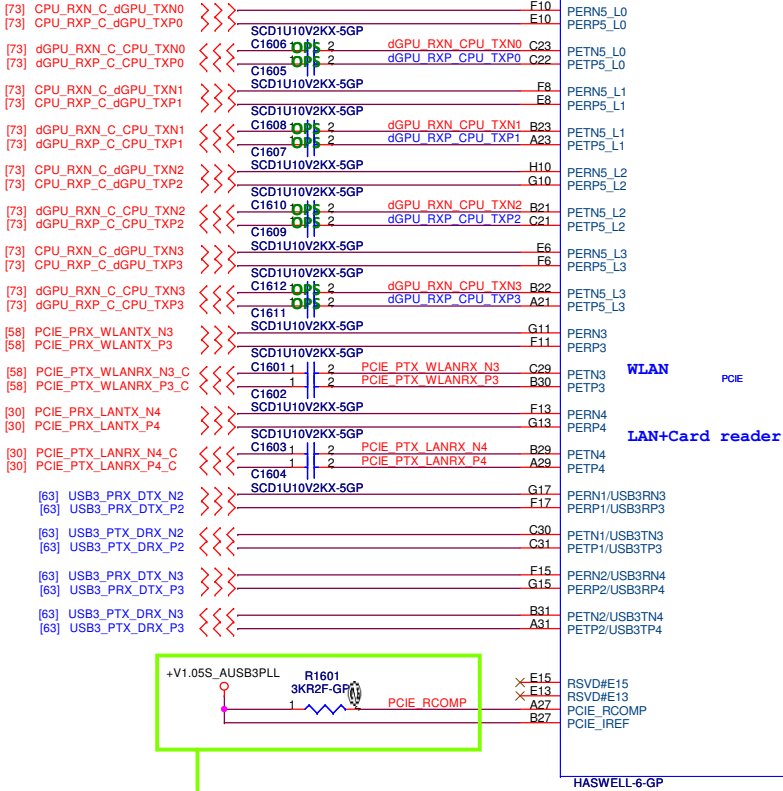
Date: Friday, June 28, 2013

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SSID = CPU

PCIE Table

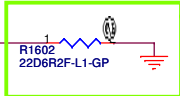
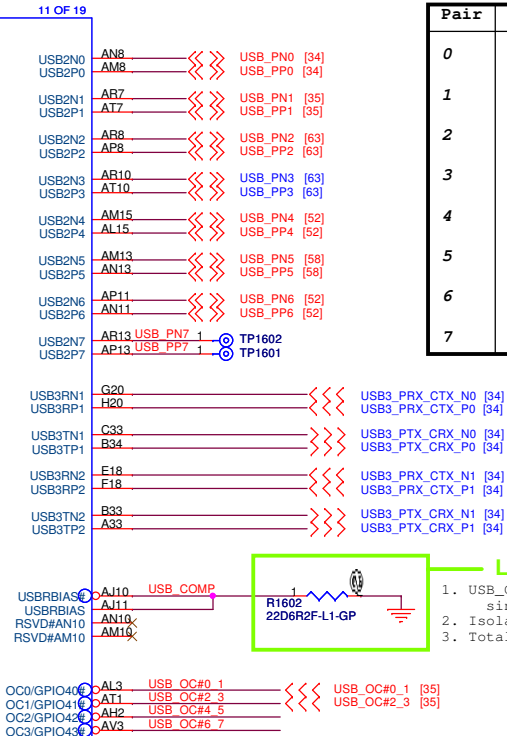
Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN+ Card reader	
5 (4lane)	GPU	
6 (4lane)	N/A	SATA0~3



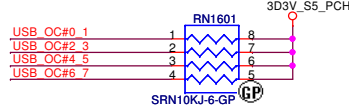
- Layout Note:
1. PCIE\_RCOMP/ PCIE\_IREF trace width=12~15mil
  2. Isolation Spacing: 12mil
  3. Total trace length<500mil

USB 2.0 Table

Pair	Device
0	USB3.0 Port2
1	USB3.0 port1 (with Power Share)
2	USB3.0 Port3
3	USB3.0 Port4
4	CAMERA
5	WLAN
6	Touch Panel
7	N/A



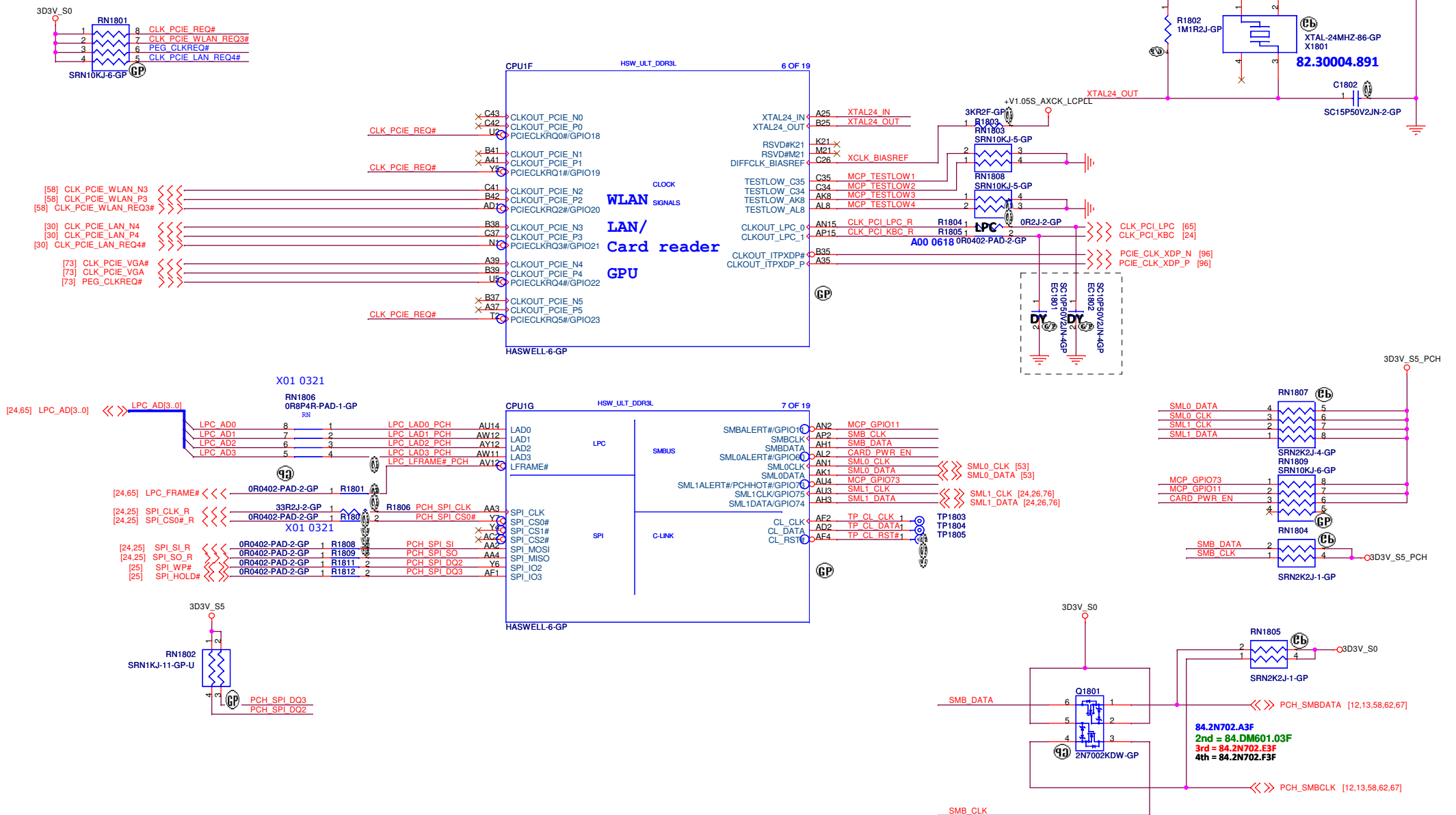
- Layout Note:
1. USB\_COMP using 50 ohm single-ended impedance
  2. Isolation Spacing :15mil
  3. Total trace length<500mil



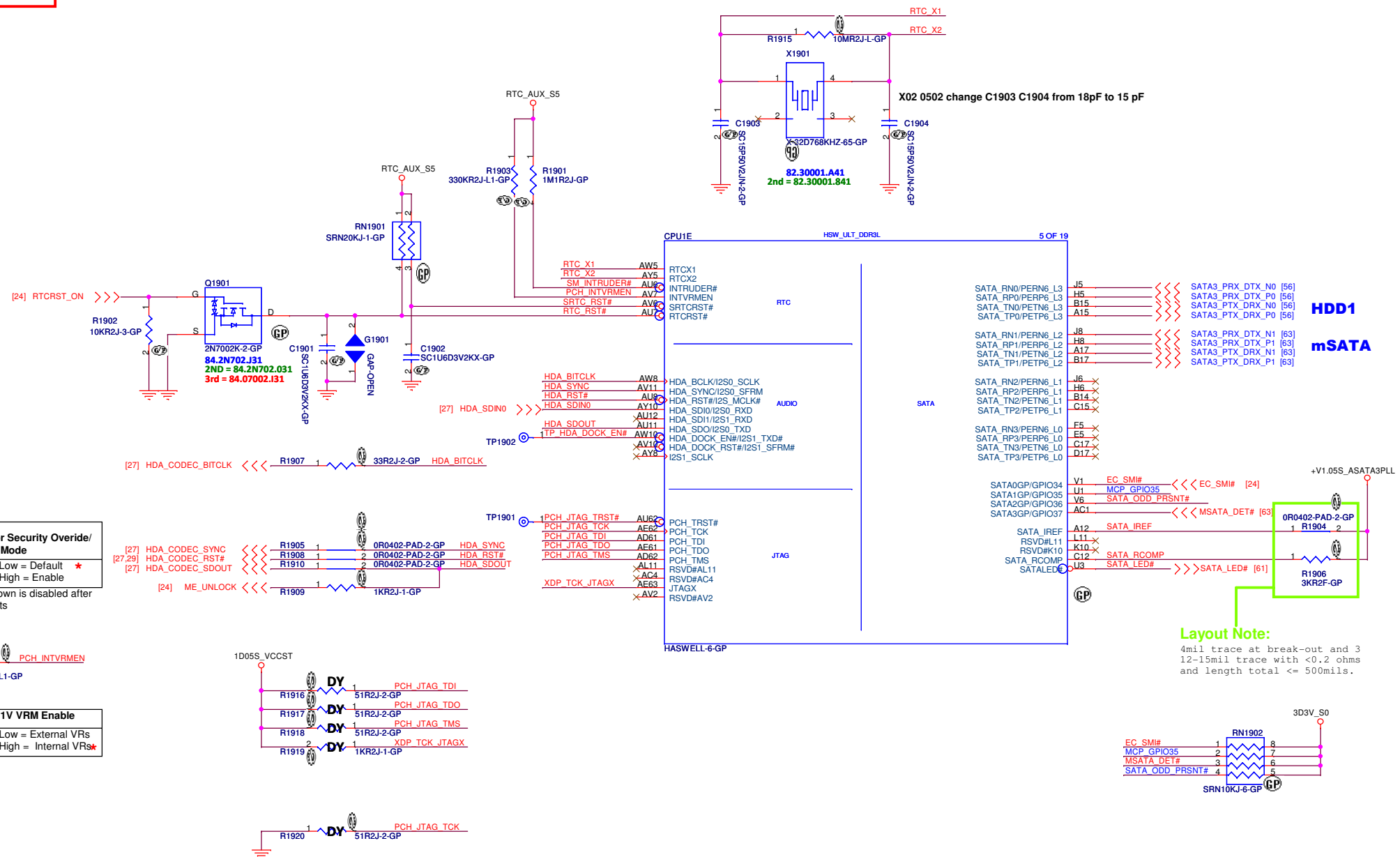




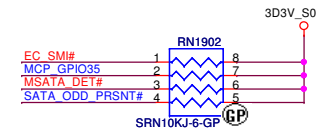
**SSID = CPU**



**SSID = CPU**



**Layout Note:**  
4mil trace at break-out and 3  
12-15mil trace with <0.2 ohms  
and length total <= 500mils.



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### **CPU (RTC/SATA/HDA/JTAG)**

Size

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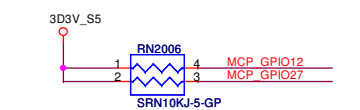
**Hadley 15"**

Rev

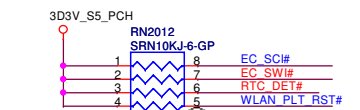
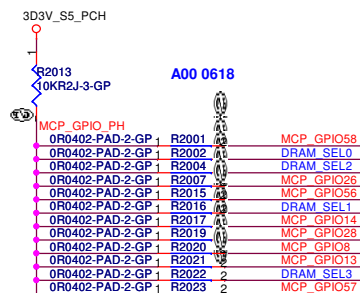
Date: Friday, June 28, 2013

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# SSID = CPU

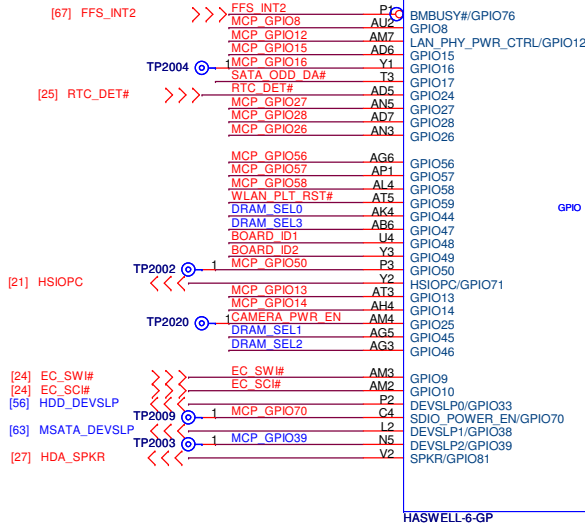
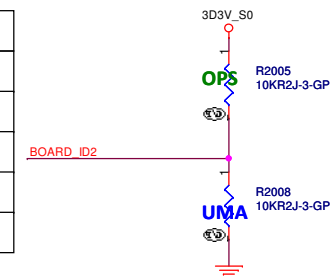


GPIO[47:44]=[1,1,1,1] for SODIMM configuration



## BIOS strap pin:

BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
PX(AMD)	0	0
DIS	0	1
UMA	1	0
Optimus(NV)	1	1



## PCH strap pin:

NO REBOOT	
HDA_SPKR	★ Low = Disable (Default) High = Enable

The internal pull-down is disabled after PLTRST# deasserts

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	High = Enable "Top-Block swap" mode (Default) ★ Low = Disable "Top-Block swap" mode

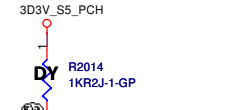
The internal pull-down is disabled after PLTRST# deasserts

TLS Confidentiality	
GPIO15	★ Low = Disable Intel ME Crypto TLS High = Enable Intel ME Crypto TLS

The internal pull-down is disabled after RSMRST# deasserts.

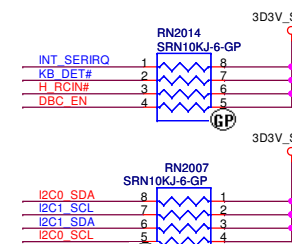
Boot BIOS Strap Bit BBS	
Boot BIOS Destination	★ Low = SPI High = LPC

The internal pull-down is disabled after PLTRST# deasserts



## Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12-15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



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Title: **CPU (GPIO)**

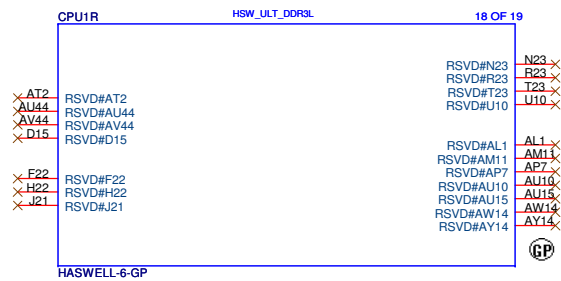
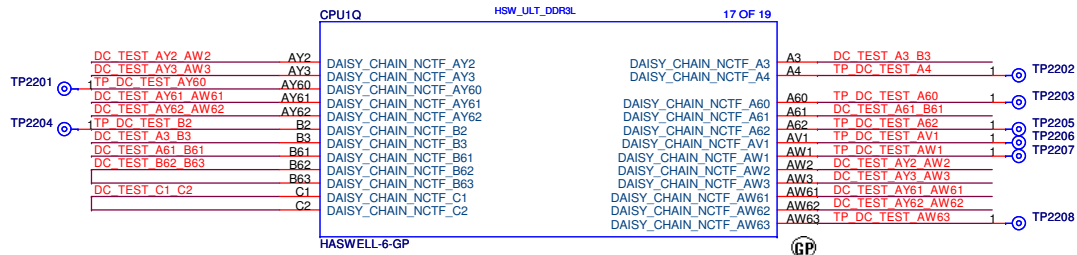
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**SSID = CPU**



SSID = CPU



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Title

**RSVD**

Size

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Document Number

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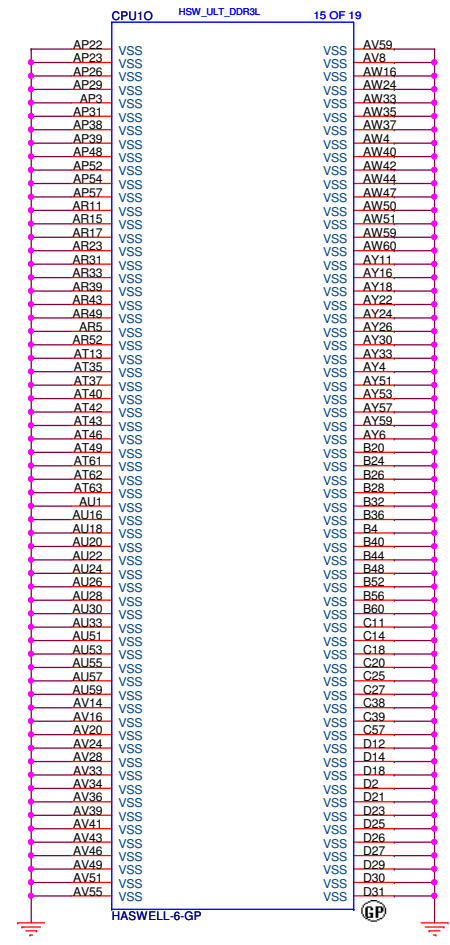
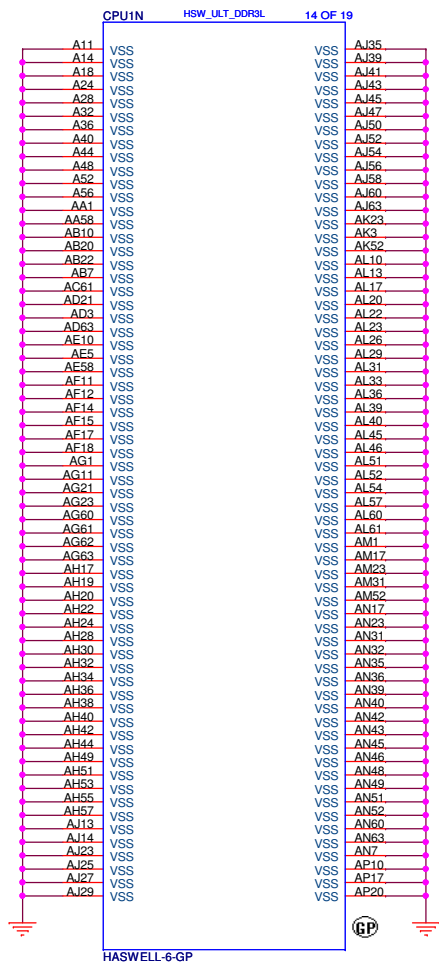
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**X02**

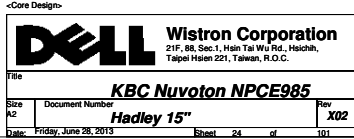
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SSID = CPU



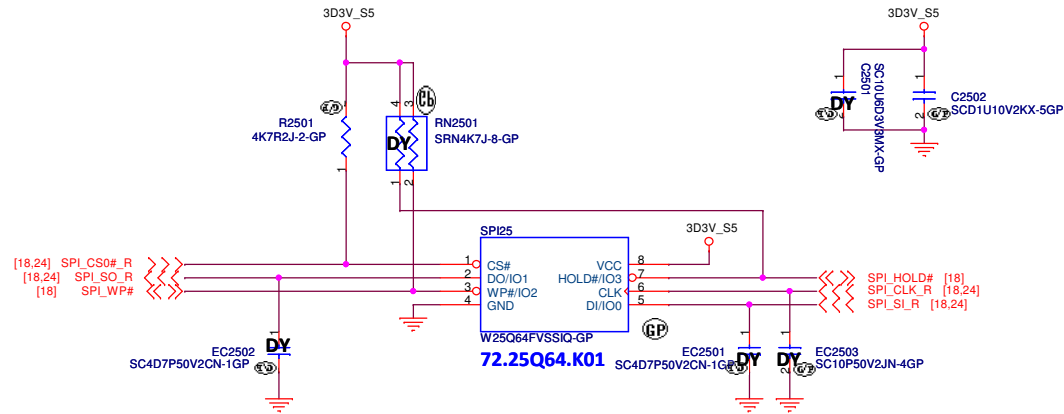
**Layout Note:**  
Need very close to EC





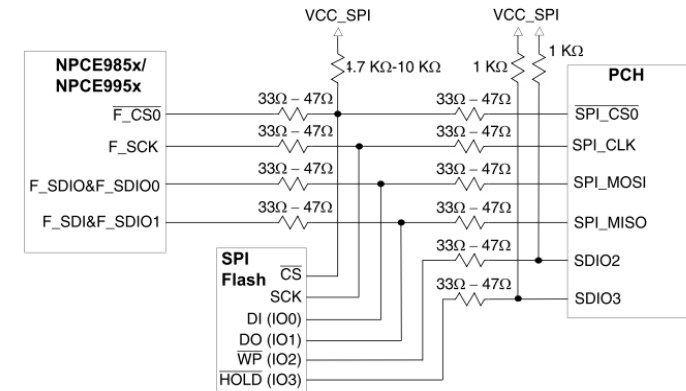
**SSID = Flash.ROM**

## SPI Flash ROM(8M) for PCH



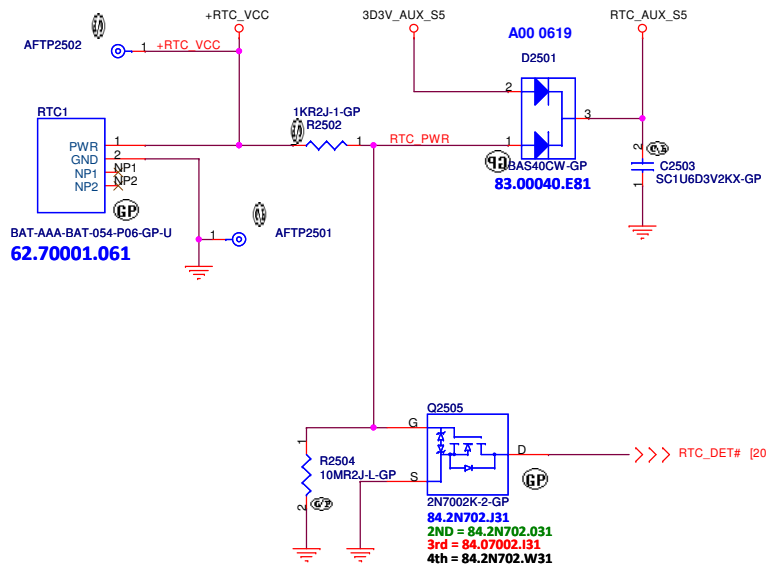
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25647.00A	O	O

### Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

**SSID = RBATT**



**<Core Design>**



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[illegible]**Flash/RTC**Size  
A3

Document Number
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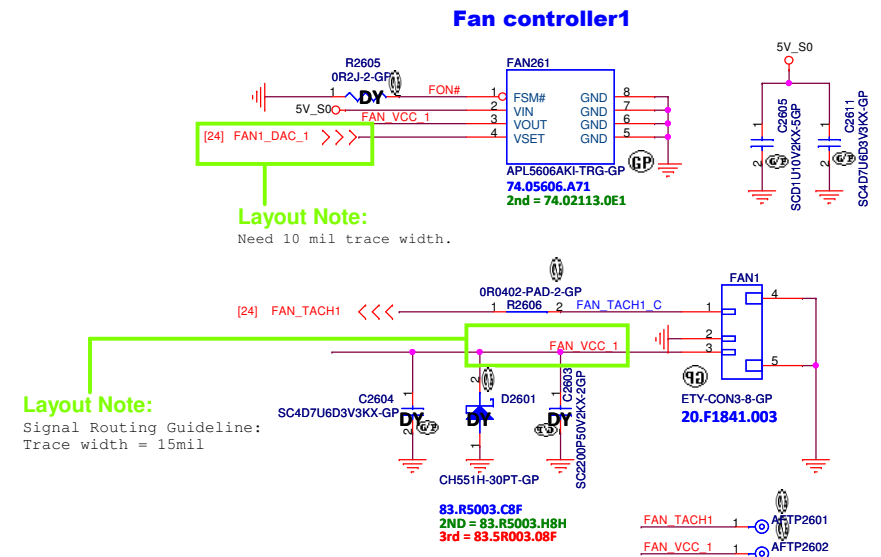
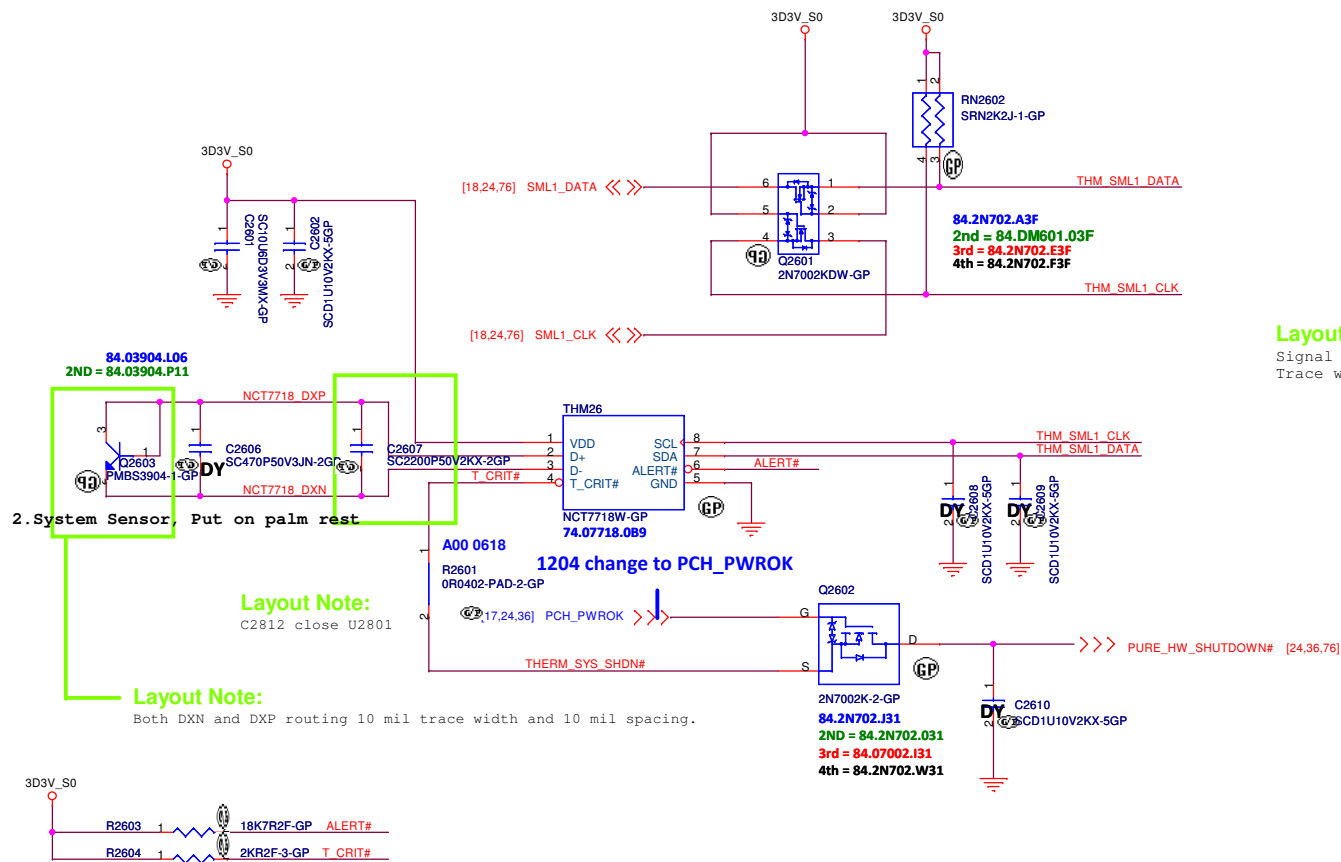
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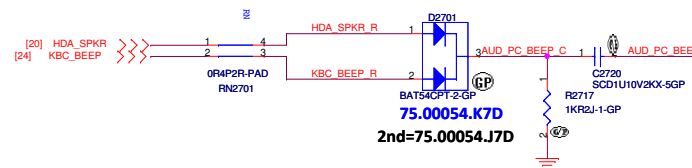
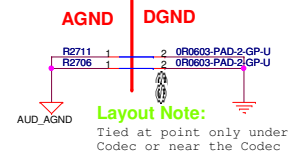
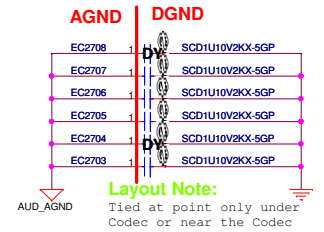
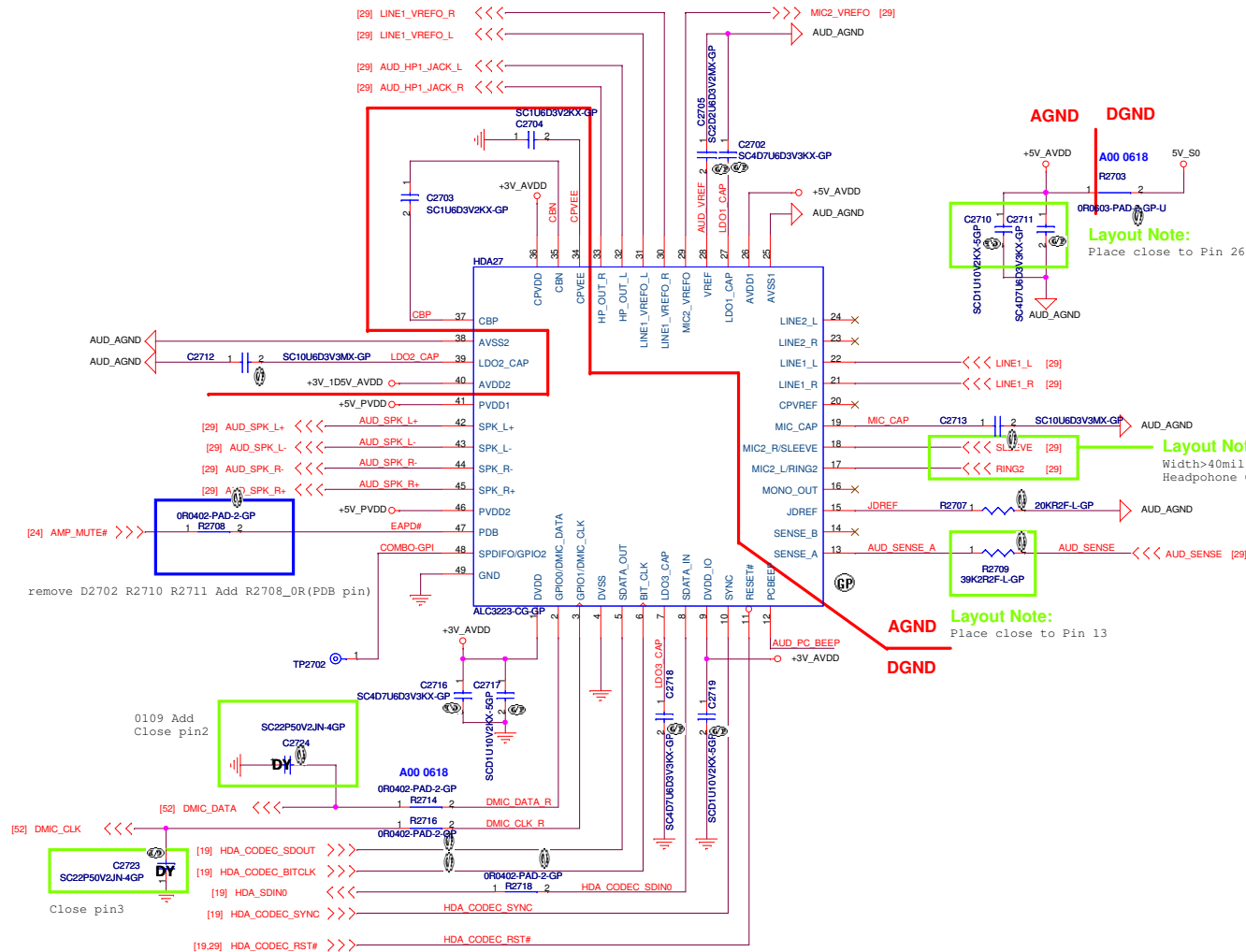
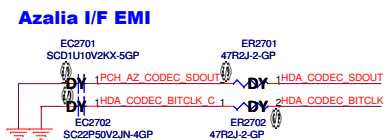
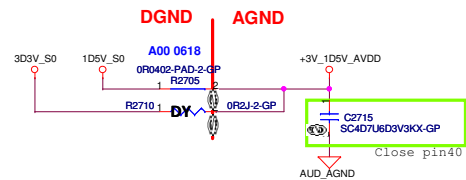
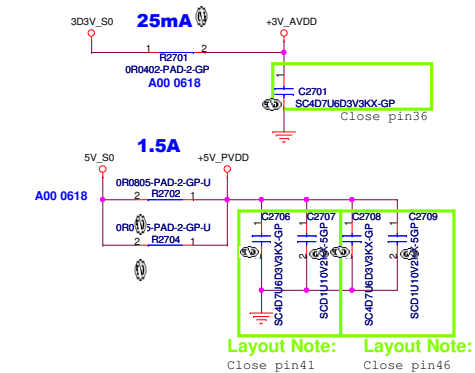
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**SSID = Thermal**




TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

SSID = AUDIO



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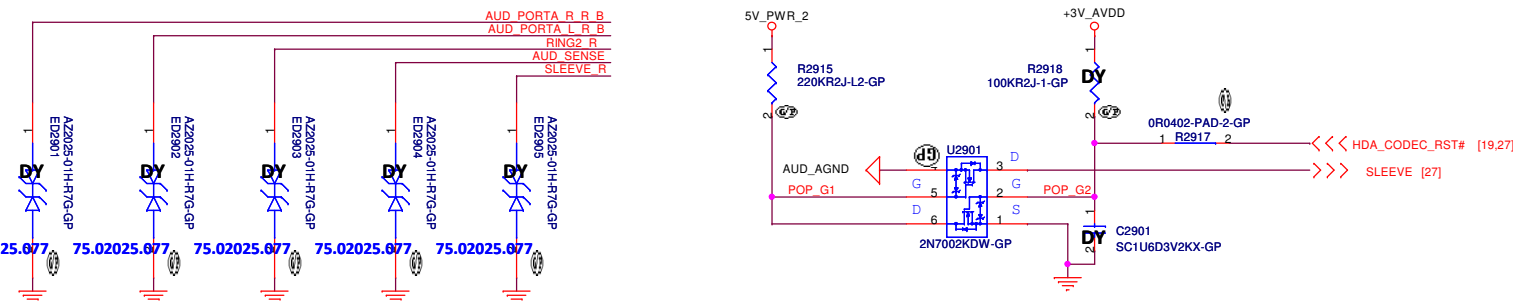
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Size  
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Rev  
**X02**

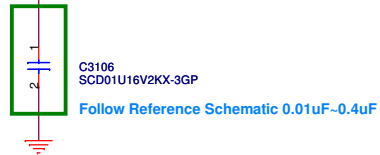
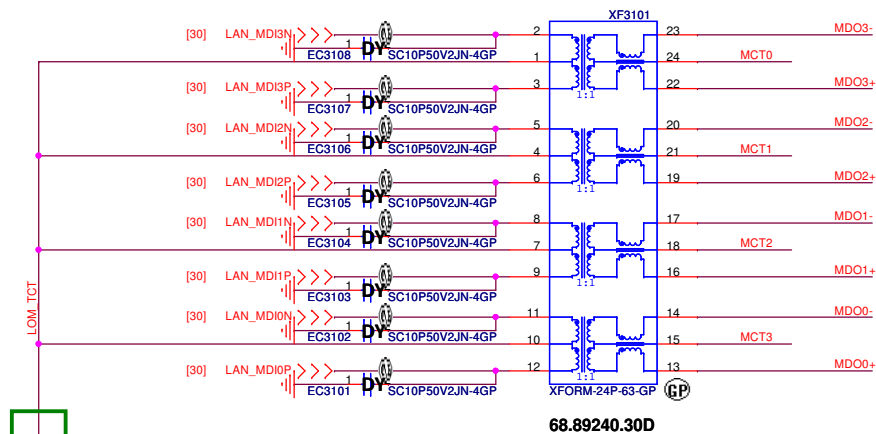
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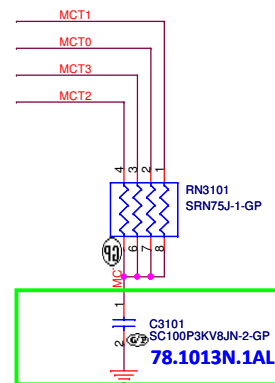


SSID = LOM

## GIGA LAN TransFormer

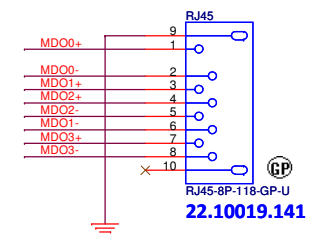
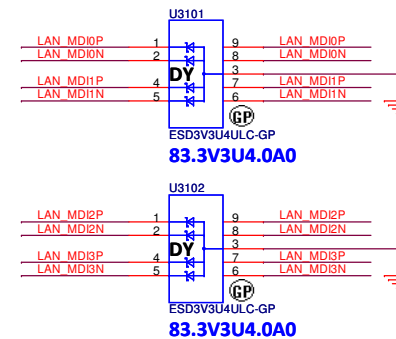


Follow Reference Schematic 0.01uF~0.4uF



Layout:  
Place near RJ45


AFTP3107	1	MDO0+
AFTP3102	1	MDO0-
AFTP3101	1	MDO1+
AFTP3103	1	MDO2+
AFTP3104	1	MDO2-
AFTP3106	1	MDO1-
AFTP3105	1	MDO3+
AFTP3108	1	MDO3-



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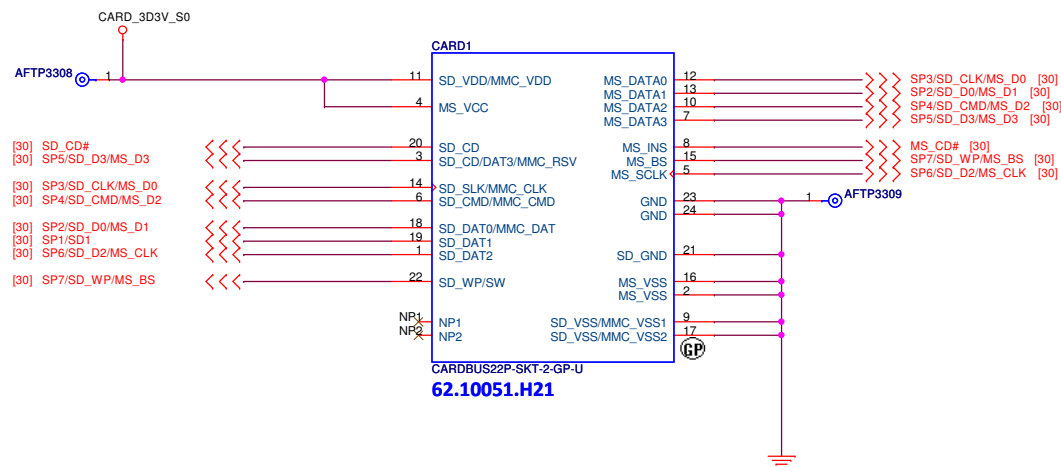
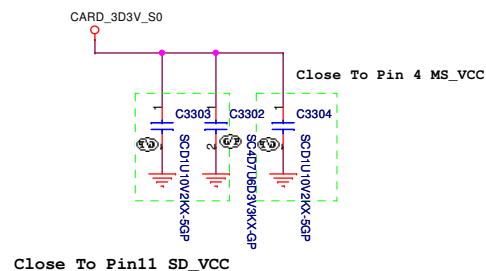
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Size	Document Number	Rev
A3	<i><b>Hadley 15"</b></i>	<i><b>X02</b></i>

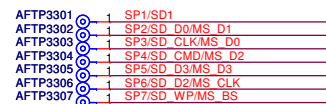
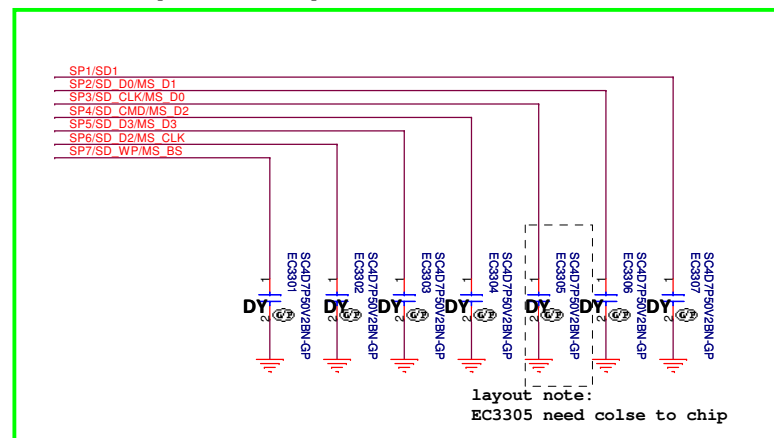
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-----------------------------	-----------------



SSID = SDIO



Reserve EMI Cap, 0107 CLK Cap DY

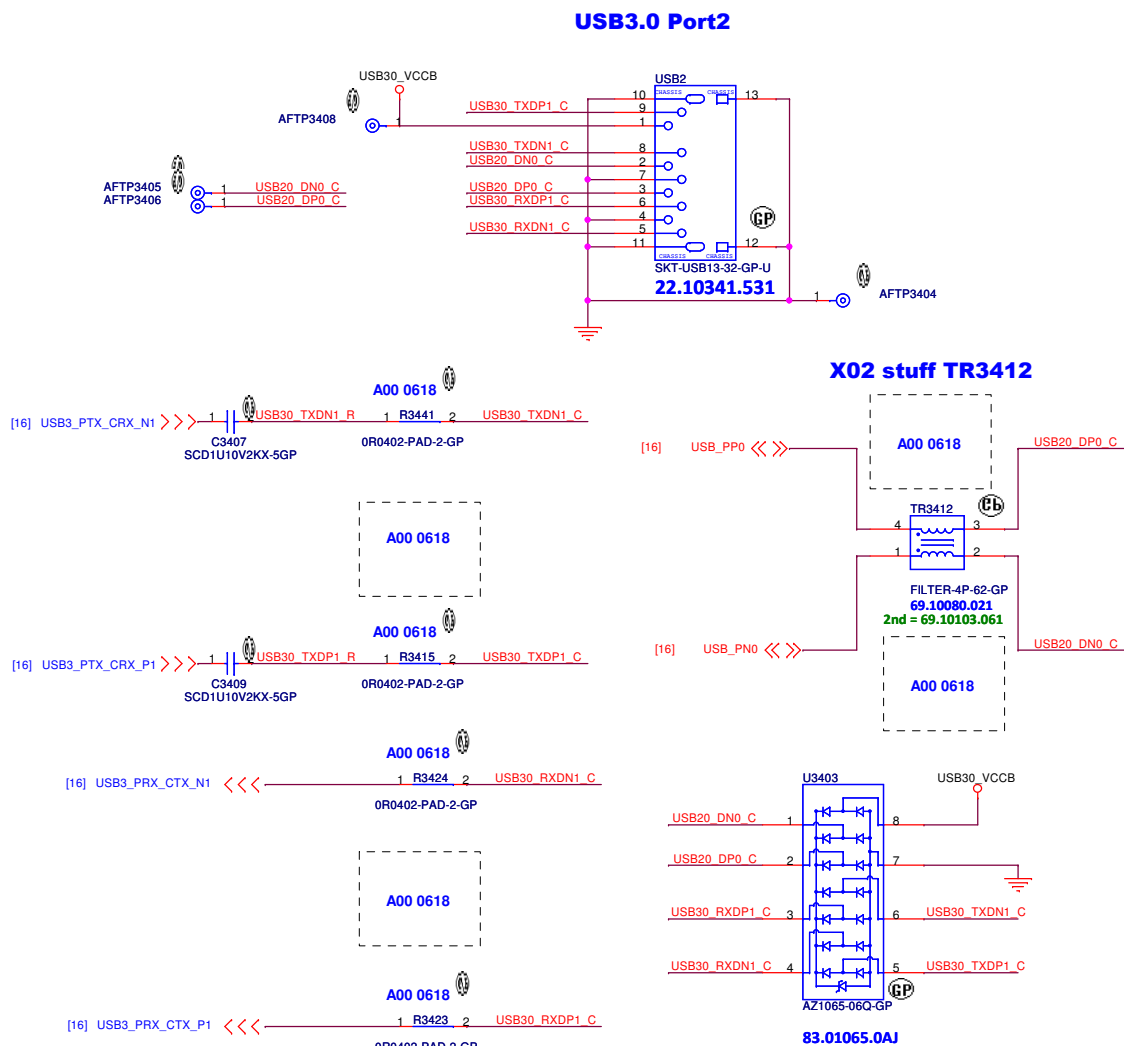
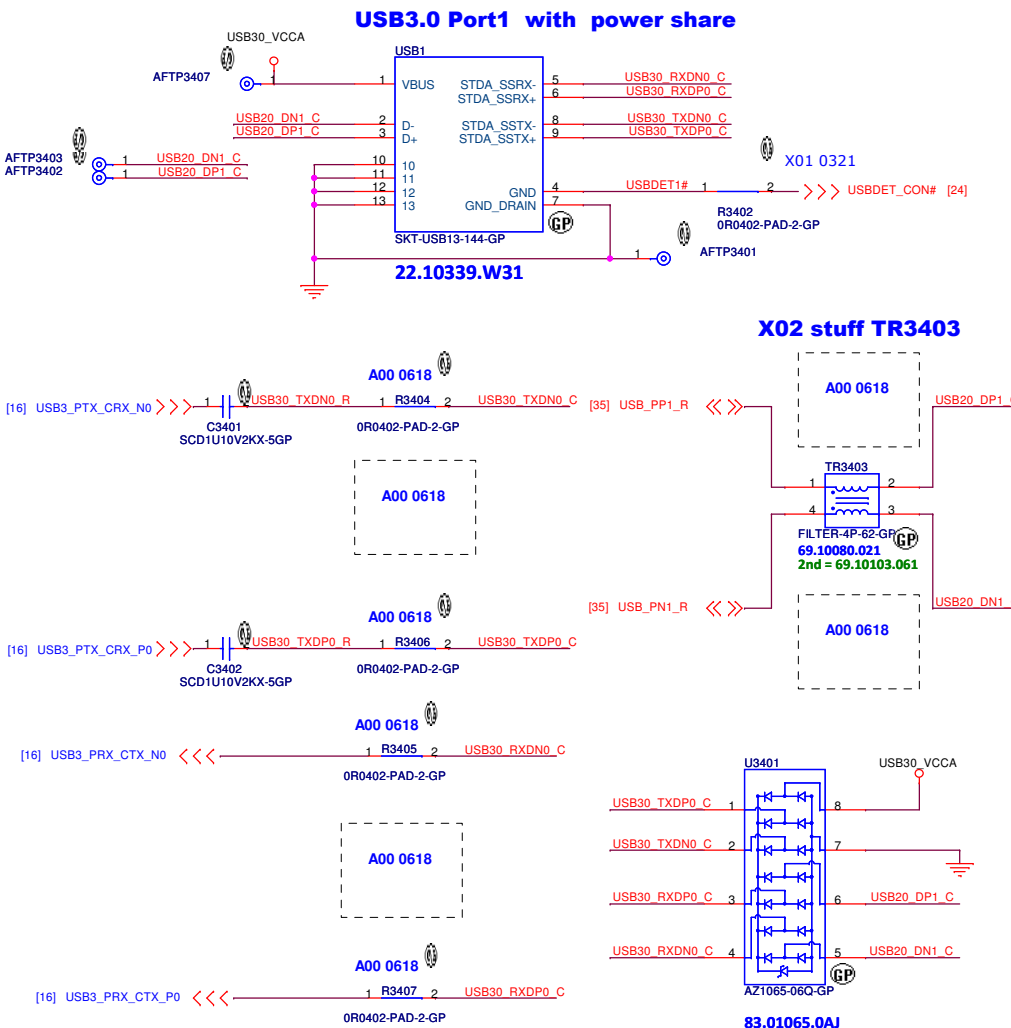


<Core Design>



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Card Reader CONN			X02
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**SSID = USB**



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Title	Author	Date	Page
1. Introduction	John Doe	2023-10-27	1-5
2. Methodology	John Doe	2023-10-27	6-10
3. Results	John Doe	2023-10-27	11-15
4. Discussion	John Doe	2023-10-27	16-20
5. Conclusion	John Doe	2023-10-27	21-25

**USB3.0(1)**

Size

Document Number

**Hadley 15"**

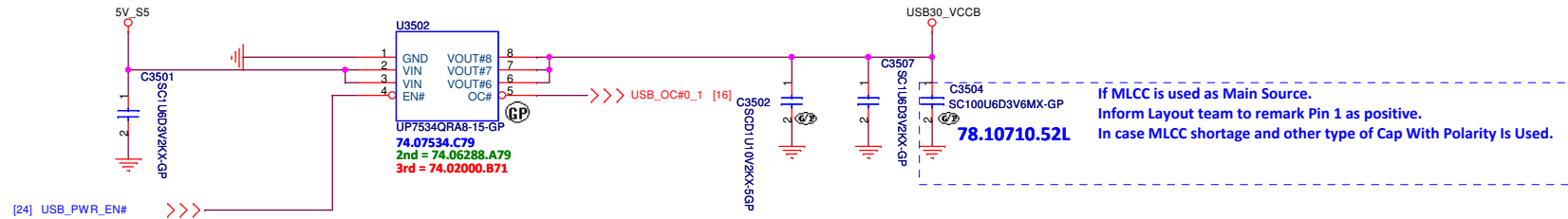
Rev

**X02**

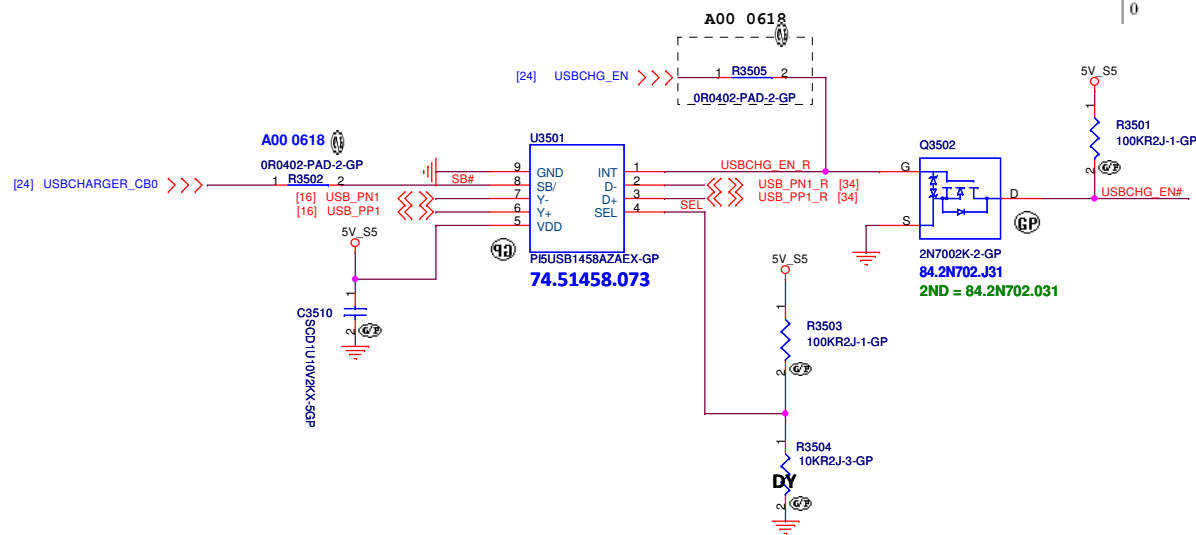
Date: Friday, June 28, 2013

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SSID = USB



### 0319 modify USB Charger circuit



#### USB Power SW (U3504)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.071	2ND
GMT	G547I2P81U	74.00547.F79	3RD

<Core Design>

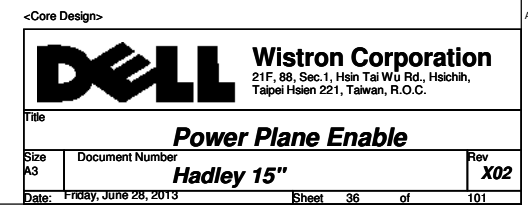
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Title: **USB Power SW**

Size: Document Number: **Hadley 15"** Rev: **X02**

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*Power Good*



SSID = Reset.Suspend

**Layout Note:**

Place Close SO-DIMMA.

**SA\_DIMM\_VREFDQ**  
**SODIMM1**

M\_VREF\_CA\_DIMMA

**SB\_DIMM\_VREFDQ**  
**SODIMM2**

M\_VREF\_CA\_DIMMB

0D675V\_VTTREF

0R2J-2-GP  
R3704

1D35V\_S3

R3706  
1K8R2F-GP

2R2F-GP  
R3708

R3703  
1K8R2F-GP

R3705  
0R0402-PAD-2-GP

C3701  
SCD022U16V2JX-GP

+V\_VREF\_PATH3

R3707  
24D9R2F-L-GP

**Close to DIMM**  
**S3 Power Reduction Circuit PM\_DRAM\_PWRGD**

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Title

**S3 Power Reduction**

Size  
A3

Document Number

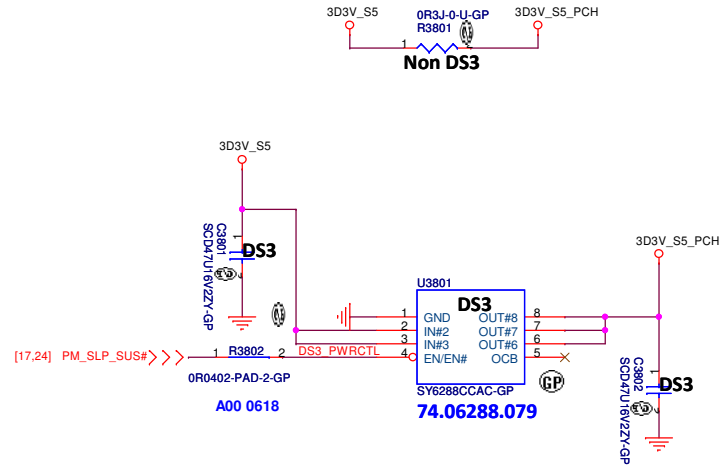
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Rev  
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SSID = Reset.Suspend



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Title

**DSW**

Size  
A3

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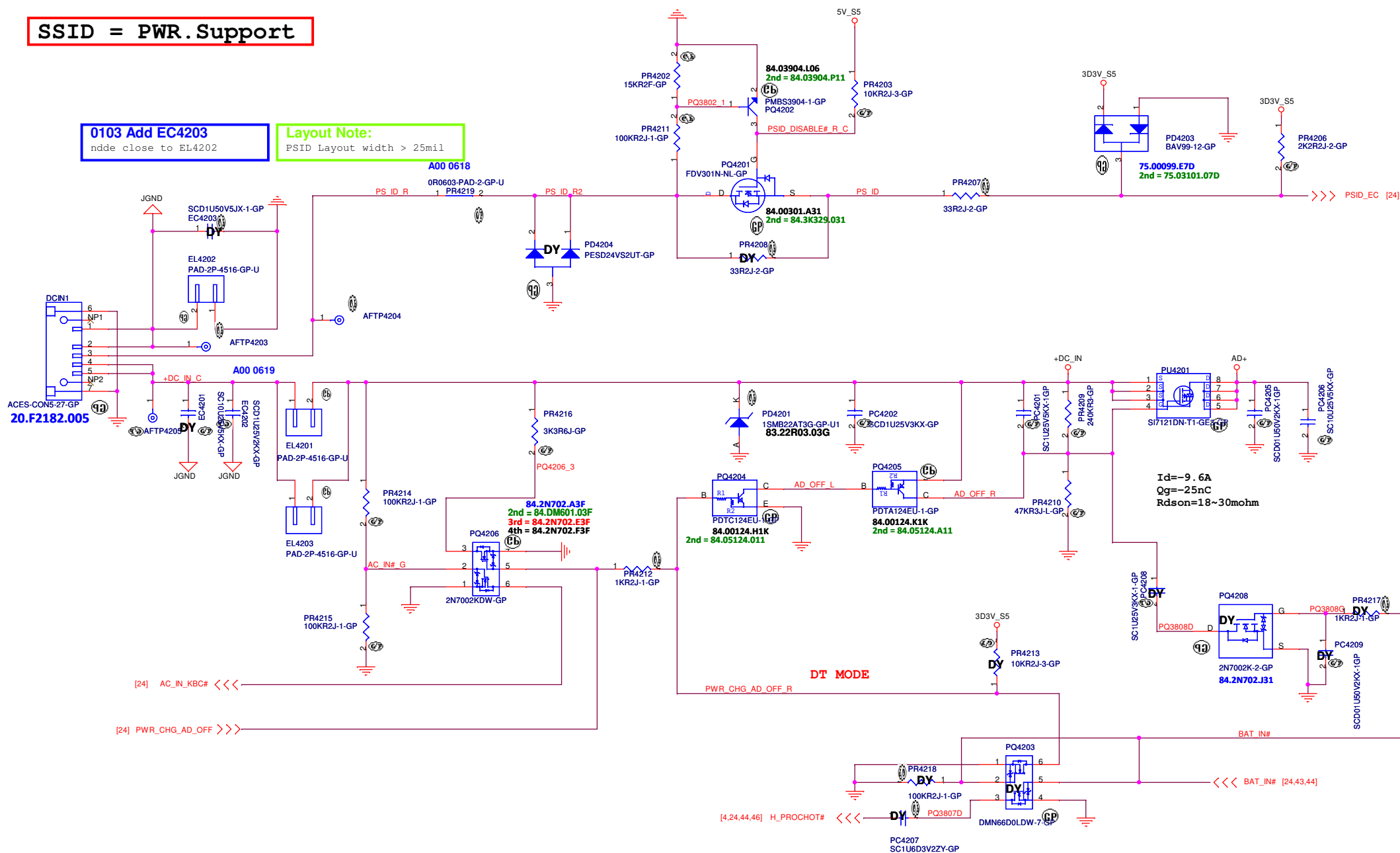
```
SSID = PWR.Support
```

0103 Add EC4203

ndde close to EL4202

**Layout Note:**

PSID Layout width > 25mil



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Title

**DCIN**

Size  
▲

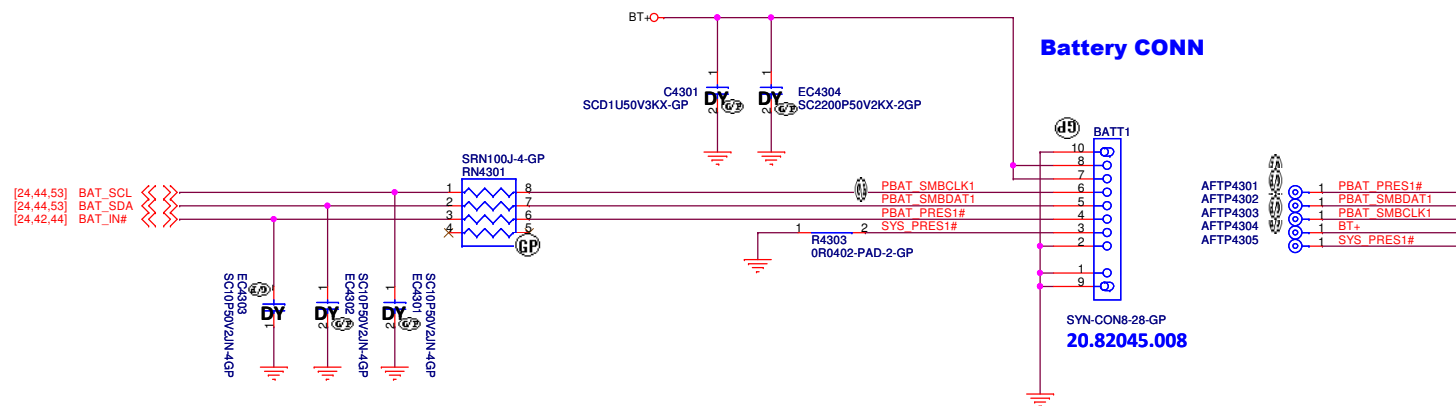
Document Number
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**Hadley 15"**

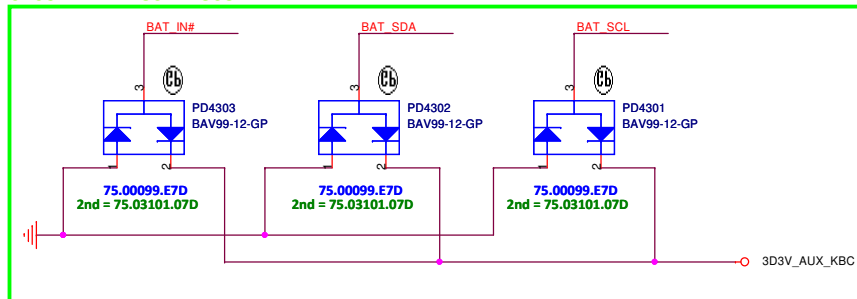
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SSID = PWR.Support



### 0109 DY PD4301~4303



### Layout Note:

Place near Battery CONN

<Core Design>

SSID = Charger

KBC FOR DT MODE  
CHECK EE PULL HIGH

DIS\_DTM:  
H= cell is plus to GND. (reset charger ic)  
L=normal

Follow customer circuits

CHECK EE

BATTERY MON

Follow customer circuits

Close PR4443

CHECK PM BATTERY TYPE  
CHECK CELL for DT mode

CHECK PM ADAPTER TYPE  
And setting adapter type

(AD\_IA\_HW)

ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
90W	L	L	1.099V
65W	H	L	0.862329V
45W	L	H	0.659648V

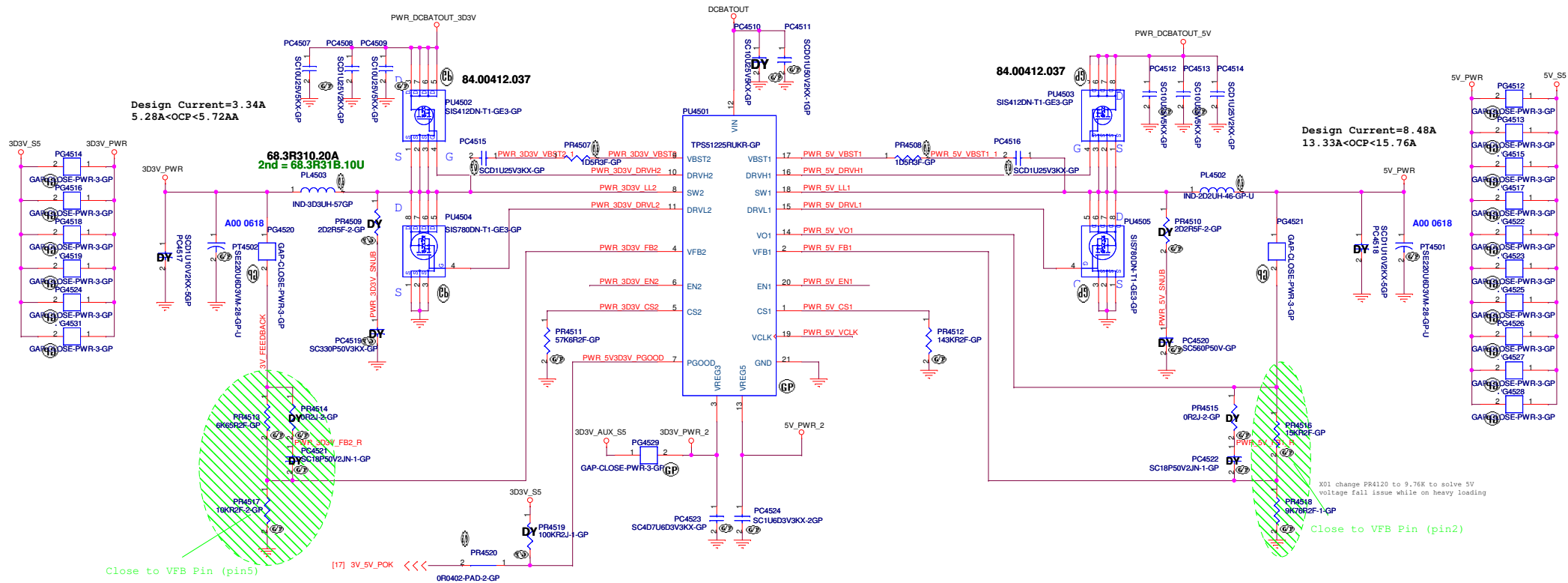
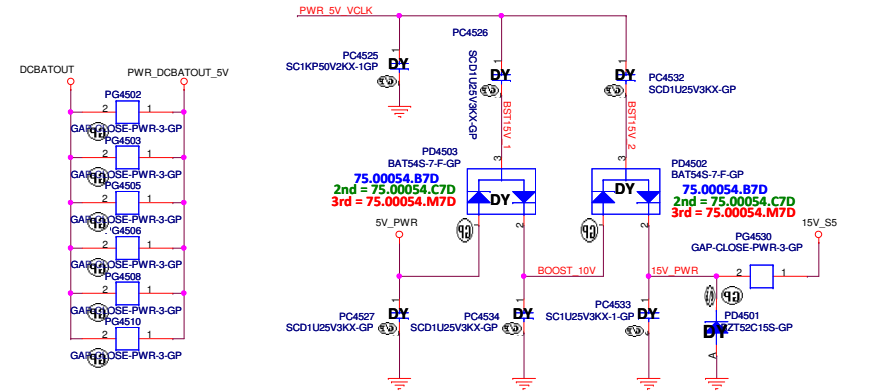
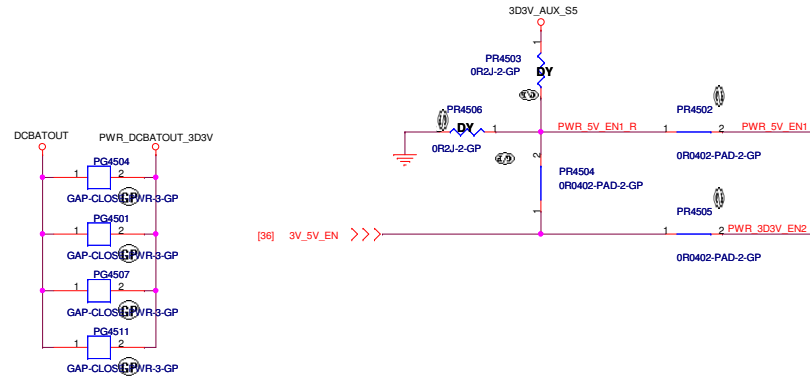
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CHARGE(BQ24715)

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```
SSID = PWR.Plane.Regulator_5v3p3v
```



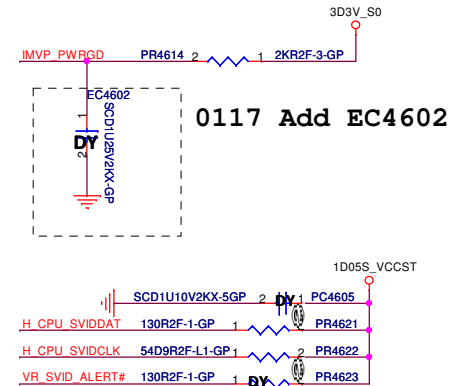
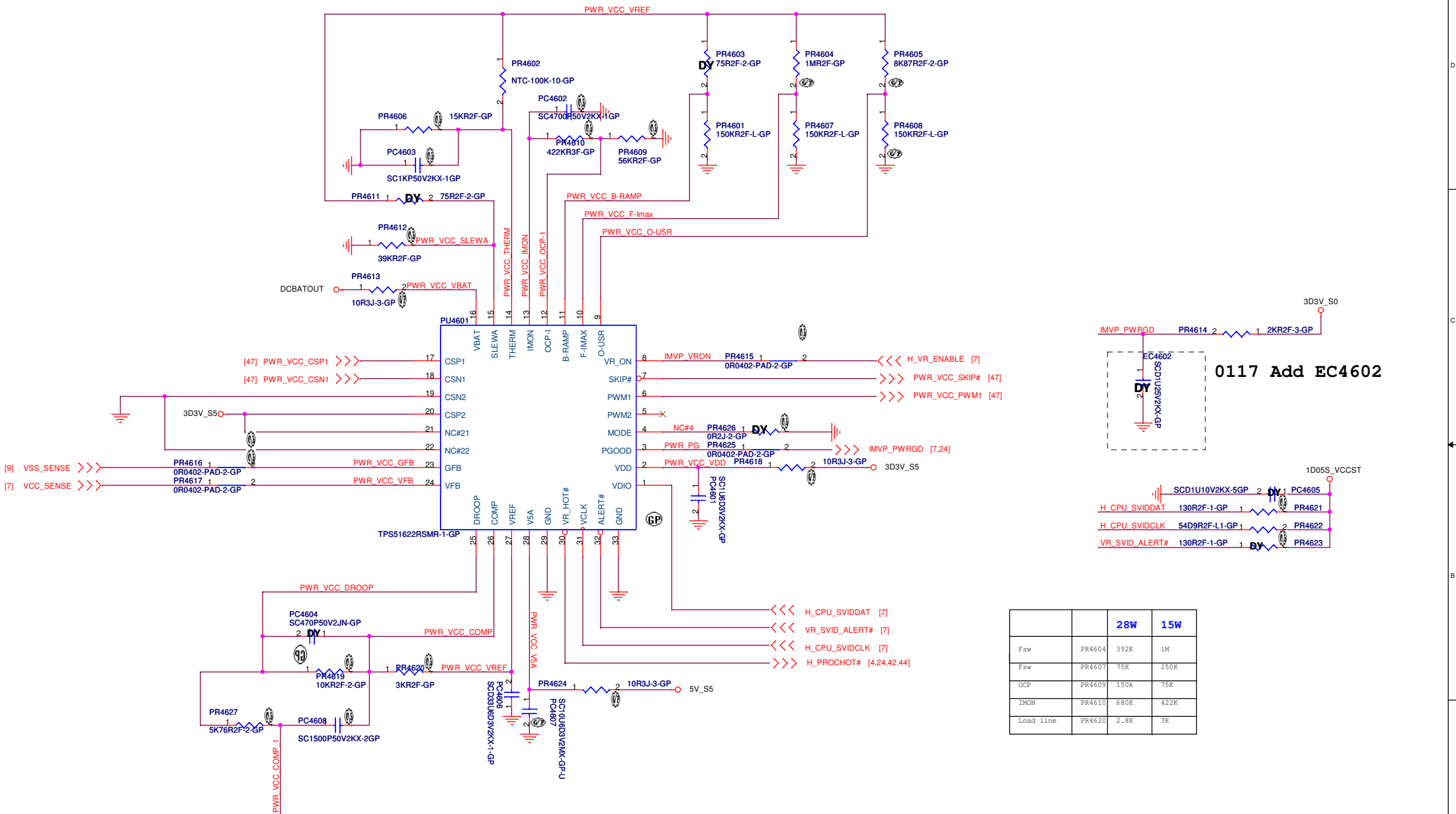
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Title				<b>3V/5V TPS51225</b>			
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SSID = CPU.Regulator



		28W	15W
Fsw	PR4604	392K	1M
Fsw	PR4607	75K	150K
OCF	PR4609	150K	75K
IMON	PR4610	680K	422K
Load line	PR4620	2.8K	3K

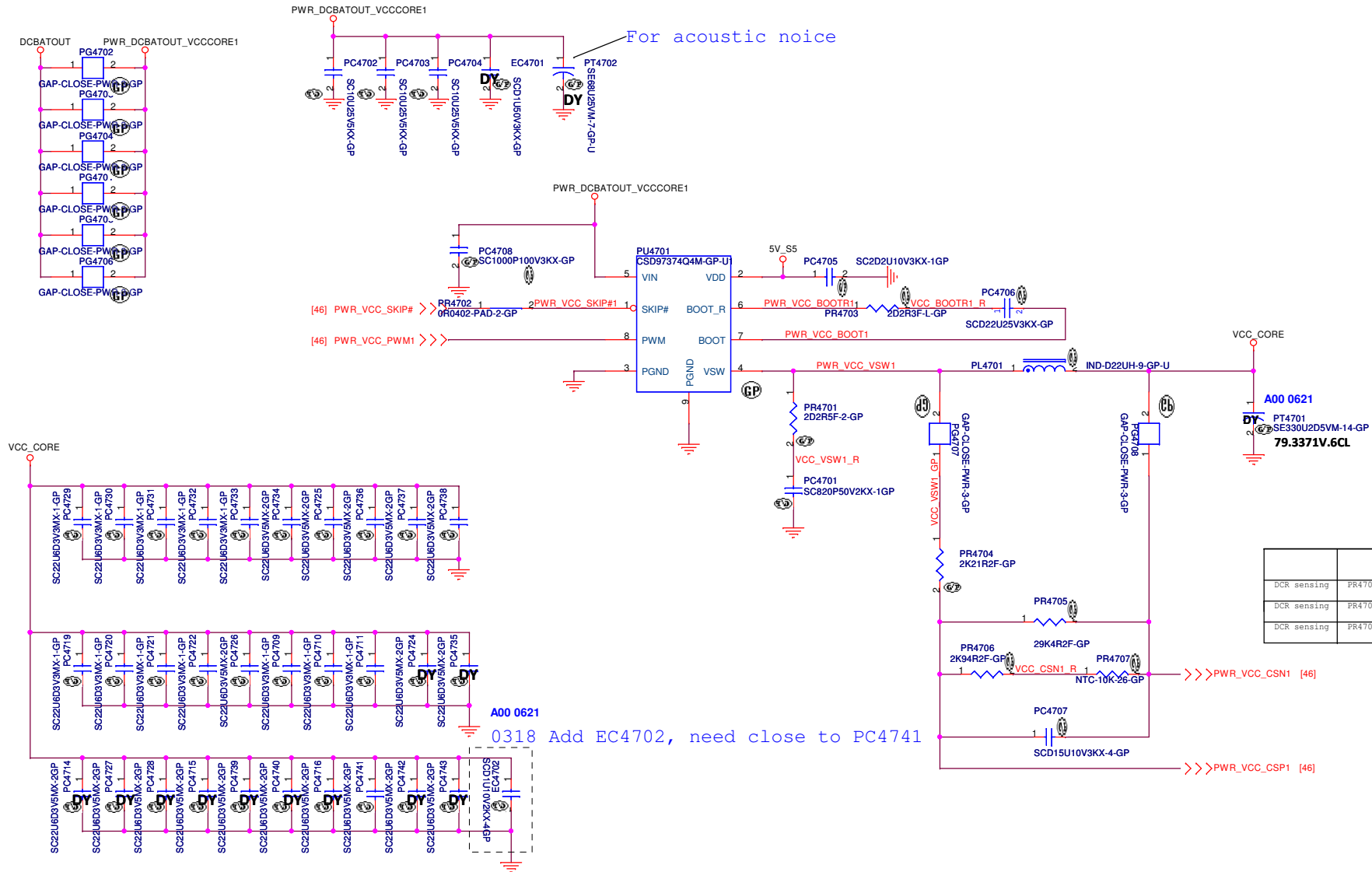
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Title			
TPS51622 CPUCORE(1/2)			
Size	Document Number		Rev
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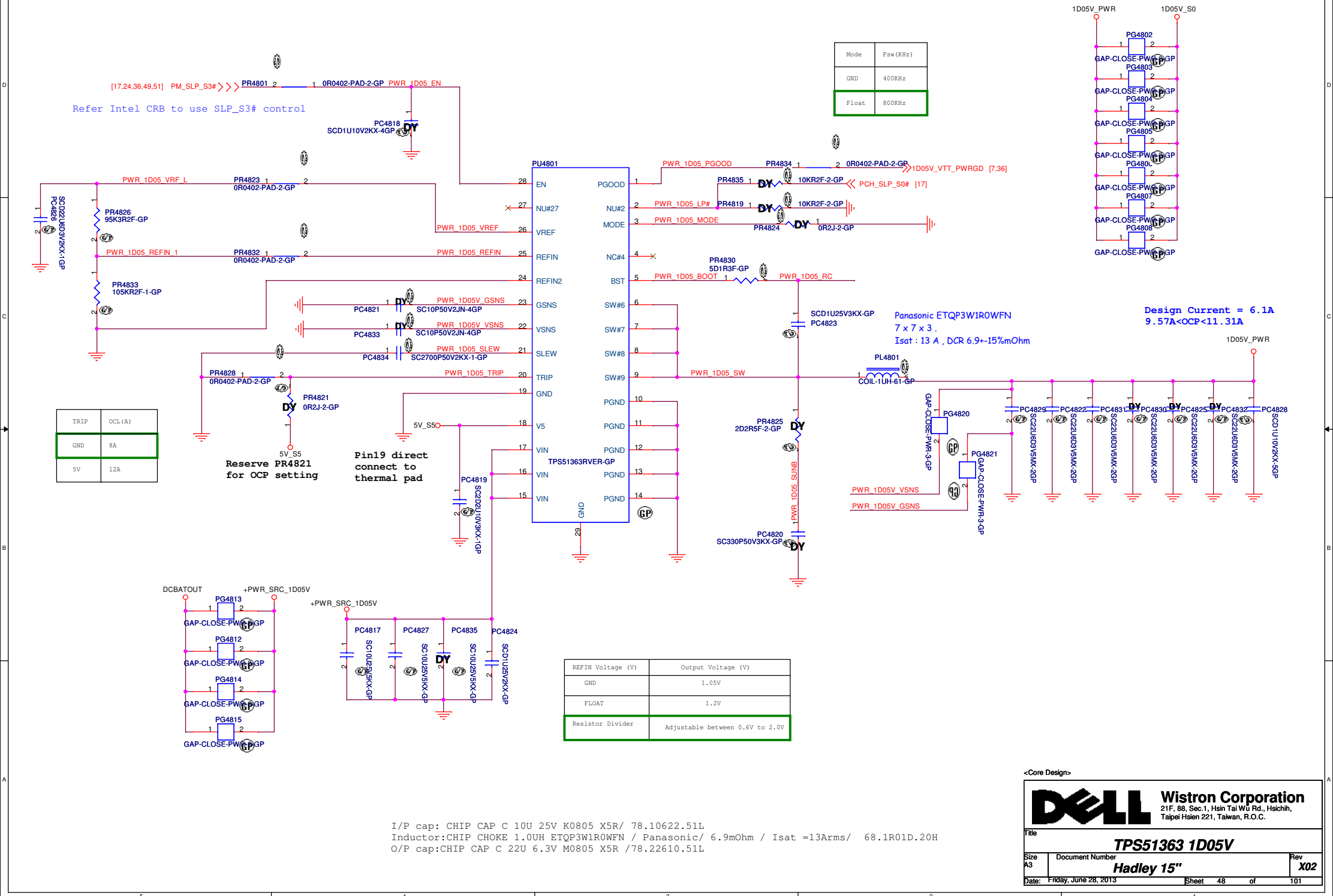
```
SSID = CPU.Regulator
```



28W CPU need stuff PC4743, PC4728, PC4739, PC4724, PC4735, PC4738

		<b>28W</b>	<b>15W</b>
DCR sensing	PR4704	2.21K	2.21K
DCR sensing	PR4706	2.94K	2.94K
DCR sensing	PR4705	60.4K	29.4K

SSID = PWR.Plane.Regulator\_1p05v



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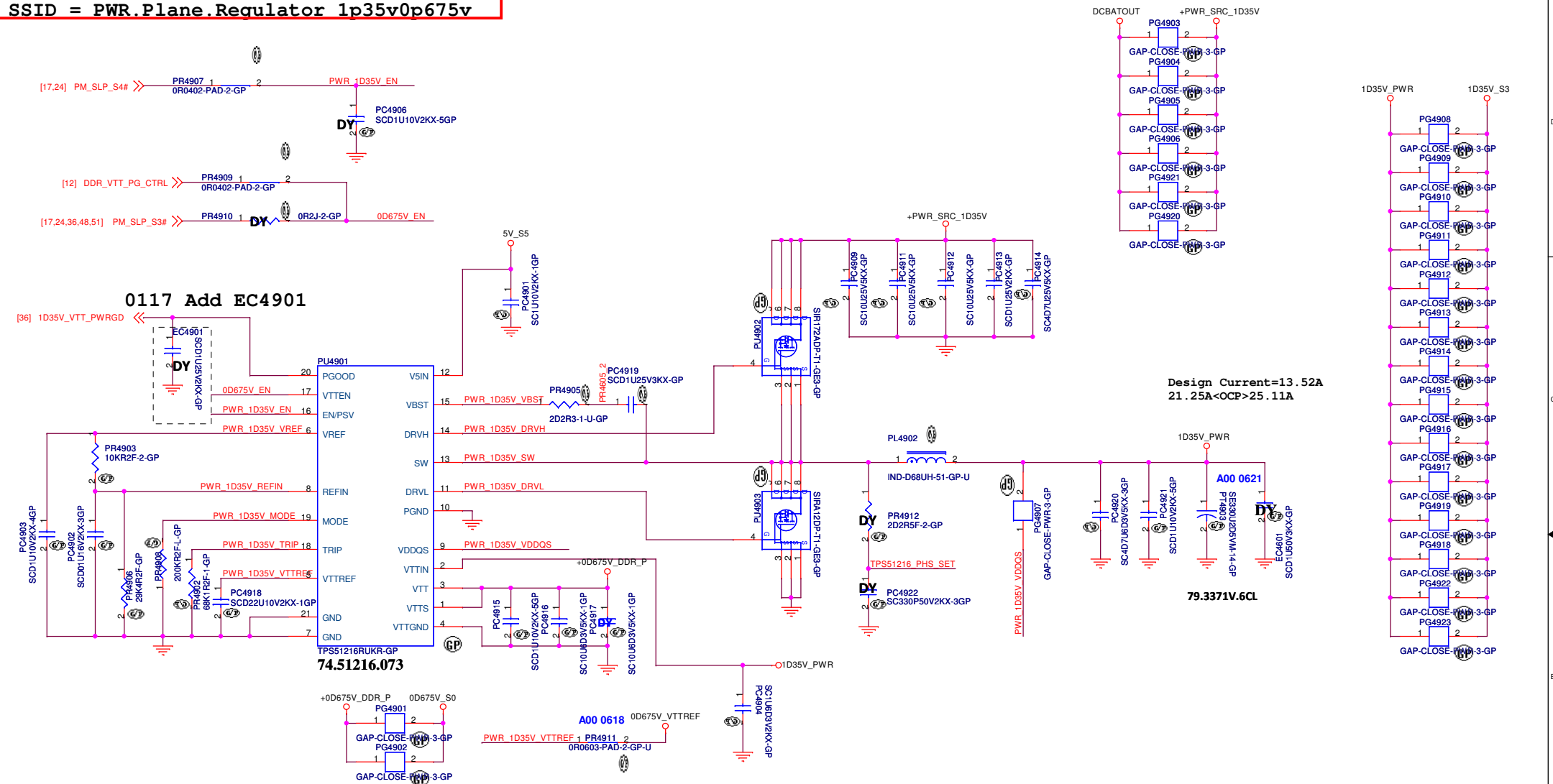
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Title: **TPS51363 1D05V**

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# SSID = PWR.Plane.Regulator 1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	Frequency	Discharge Mode
PR4608	400kHz	Tracking Discharge
200k ohm	400kHz	
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKE 1.0UH PCMB104T-1R0M/ 3.3mohm/ Isat =28A rms /68.1R01C.10Q  
O/P cap: CHIP CAP POL 330U 2.5V M 6.3\*4.5 2.3Arms Matsuti/77.53371.18L  
H/S: SIR172ADP-T1-GE3 / 8.5mohm/10.5mOhm@4.5Vgs/ 84.00172.A37  
L/S: SIR12DP-T1-GE3 / 4.4mohm/6mOhm@4.5Vgs/ 84.SRA12.037

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Title  
**TPS51216 +1.35V SUS**


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*(Reserved)***TPS51312 1D8V**

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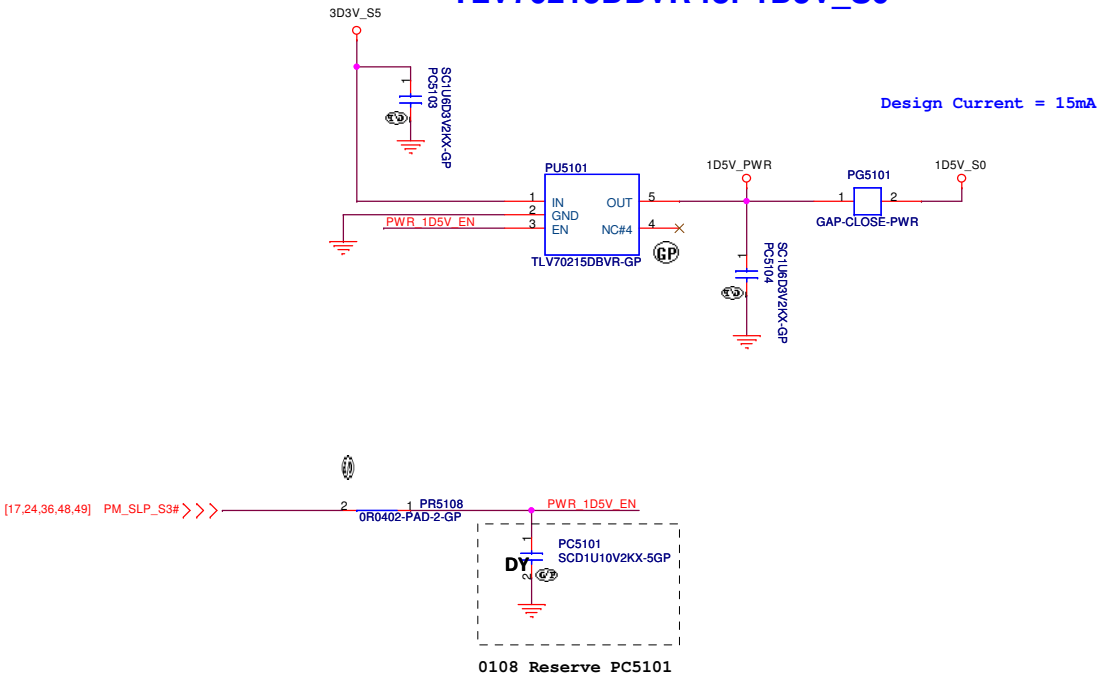
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SSID = PWR.Plane.Regulator\_1p5v

TLV70215DBVR for 1D5V\_S0



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**RT9198-15PU5R 1D5V**

Size

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**Hadley 15"**

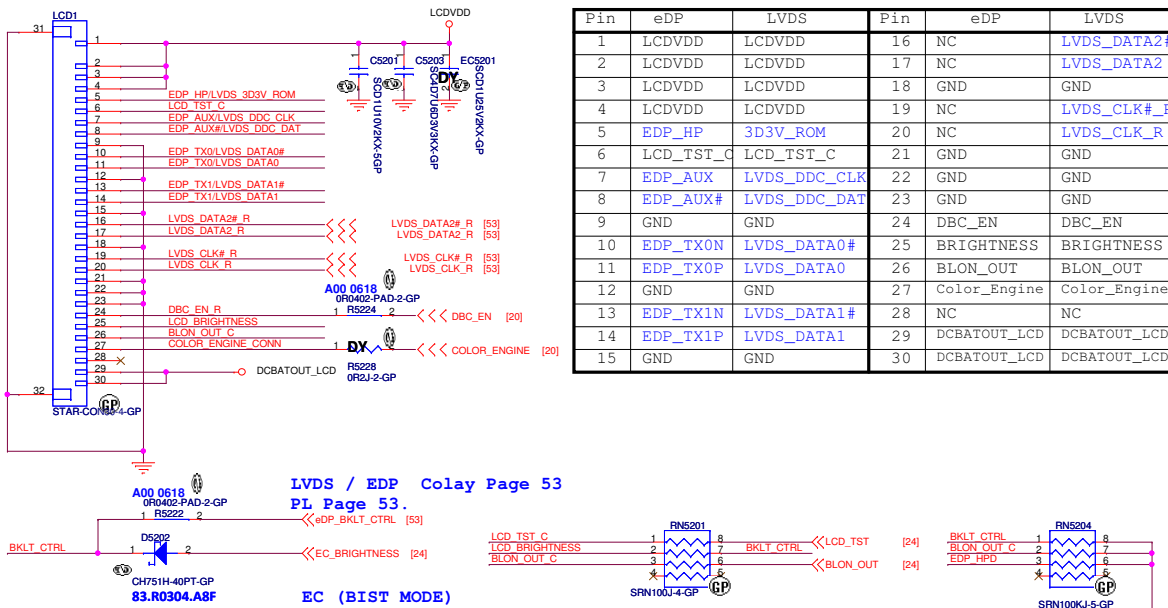
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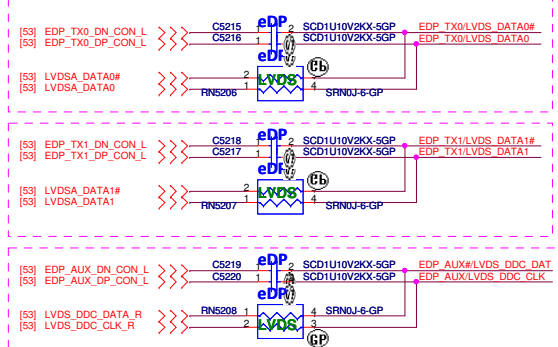
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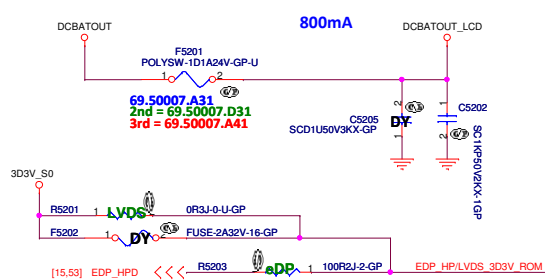
## SSID = VIDEO



### eDP/ LVDS select circuit

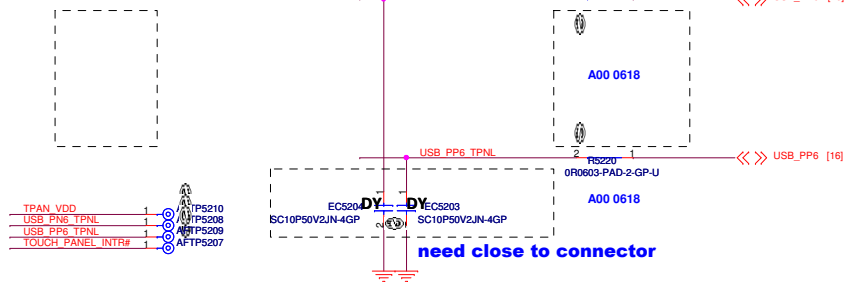


## INVERTER POWER

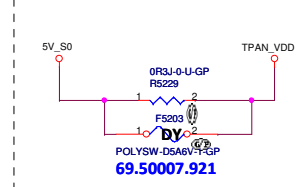


## Touch panel

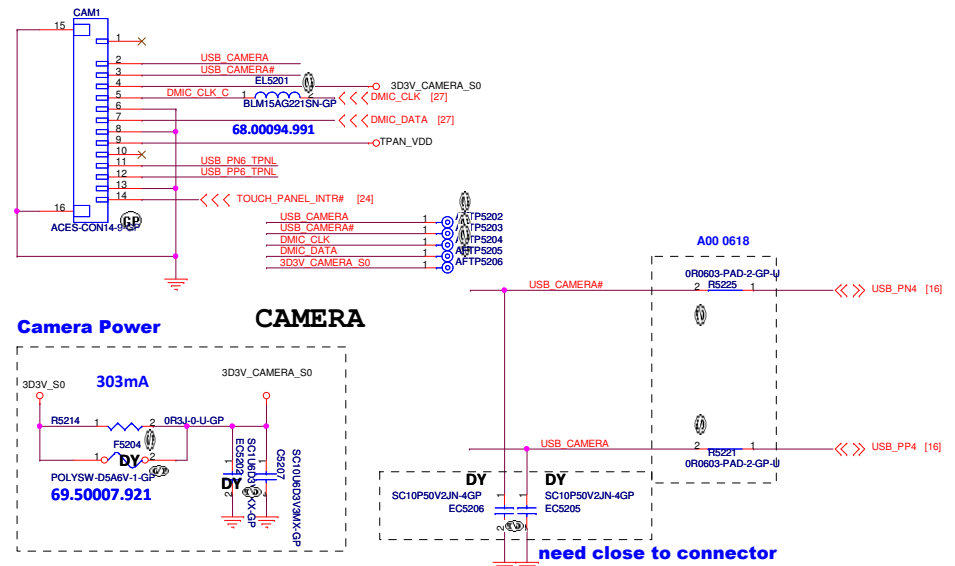
## X02 remove TPNL1



0307 modify

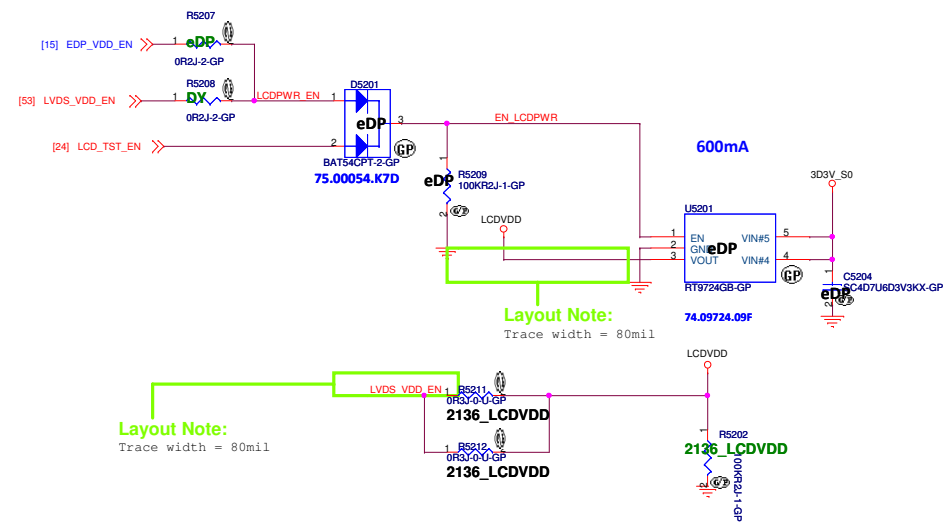


## X02 change CAM1 connector



LCDVDD

## LCD Power



**<Core Design>**

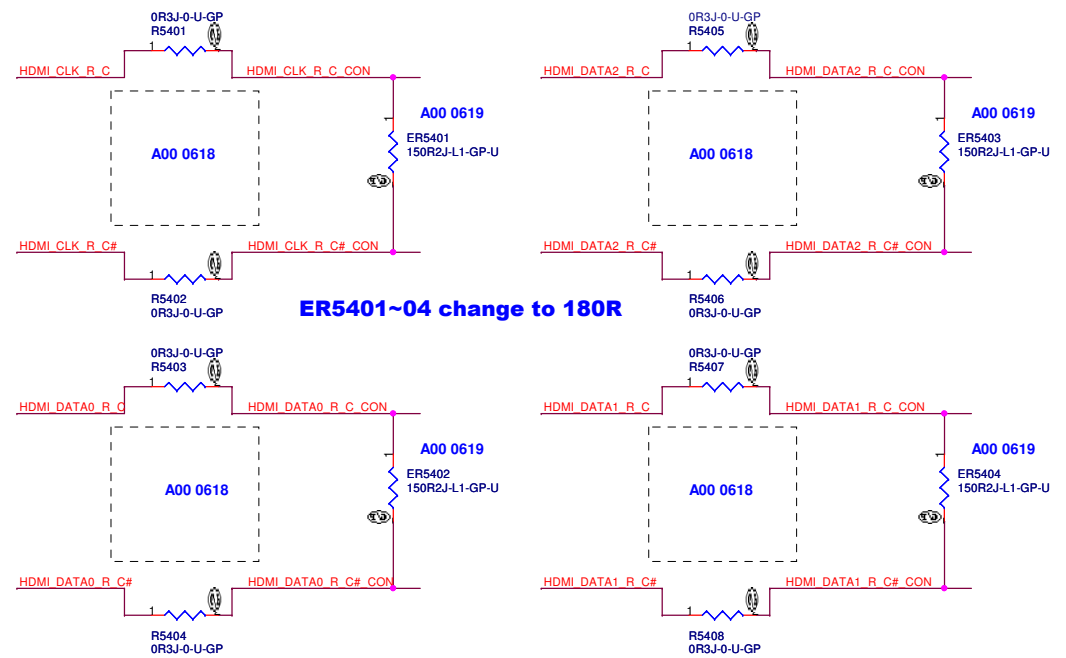
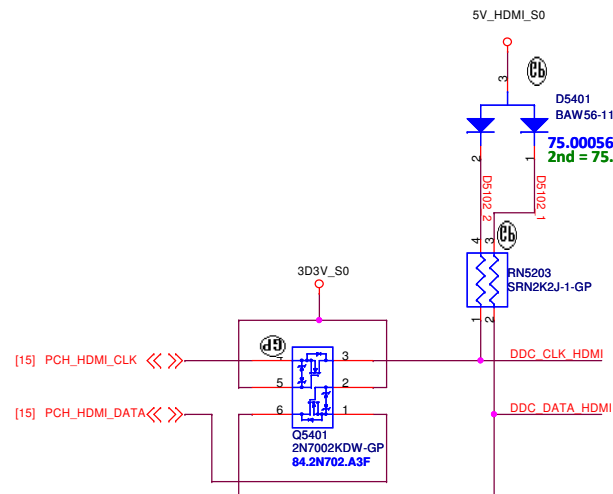
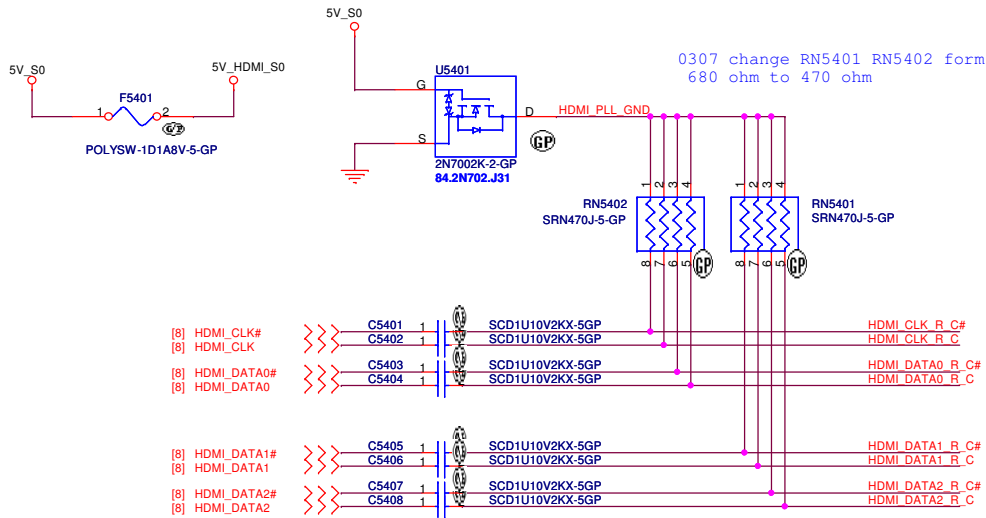


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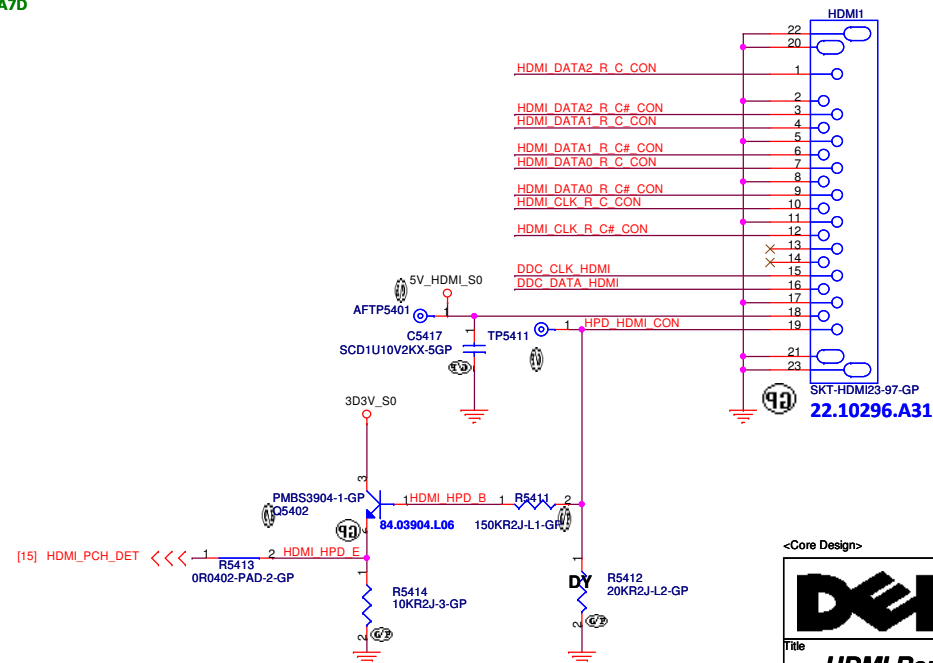
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<b>LCD Connector</b>			
Size Custom	Document Number		Rev
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# SSID = VIDEO



## HDMI CONN



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Title		
HDMI Repeater/Connector		
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Title

Size  
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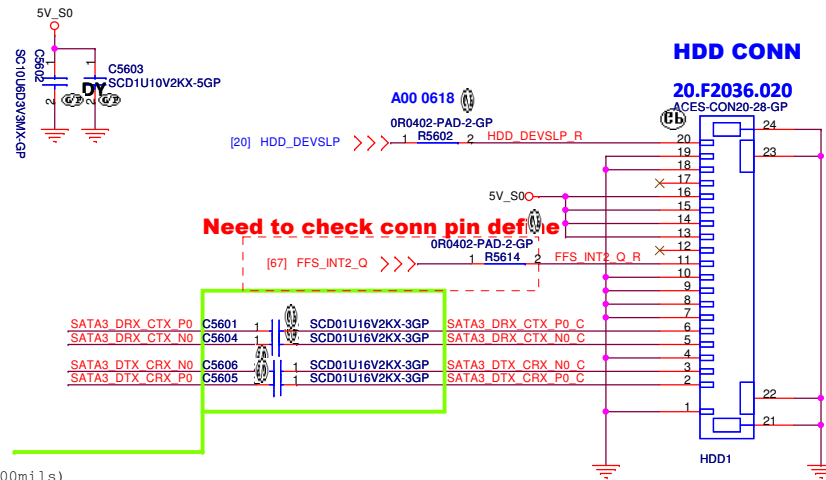
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Rev  
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SSID = SATA



**Layout Note:**

AC coupling Cap;  
place near CONN(<100mils)

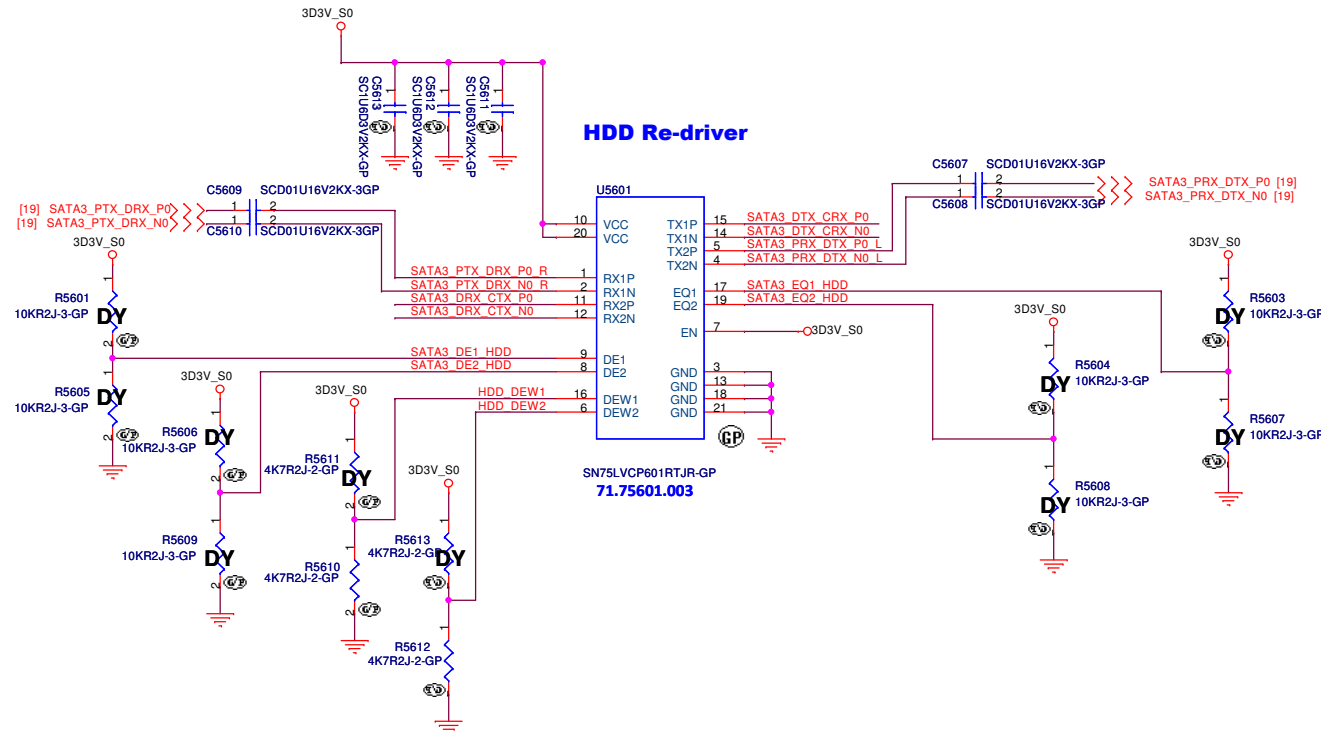


Table 1: Tx/Rx EQ & DE Pulse Width Settings

DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps)
NC (default)	-6
0	0
1	-3

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)
NC (default)	0
0	7
1	14

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

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Title <b>HDD</b>		
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Title

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A3

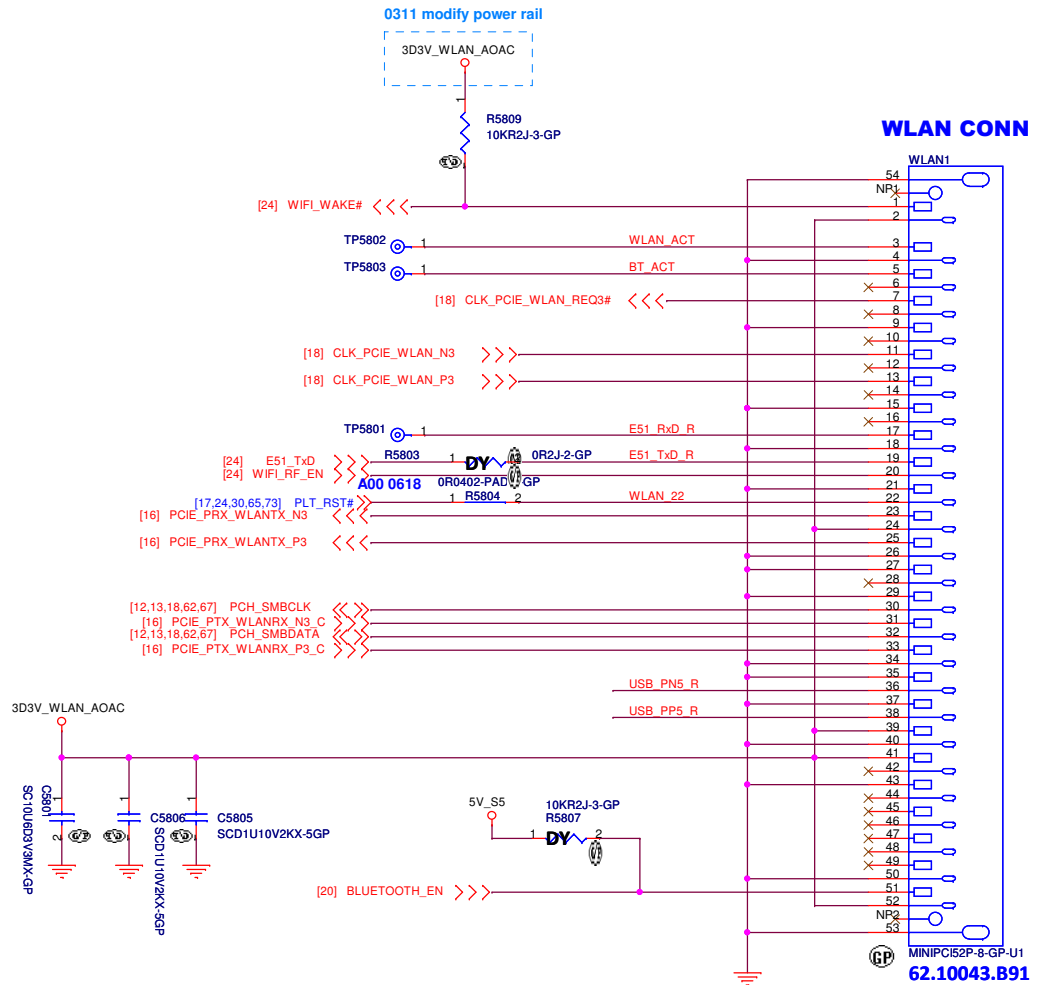
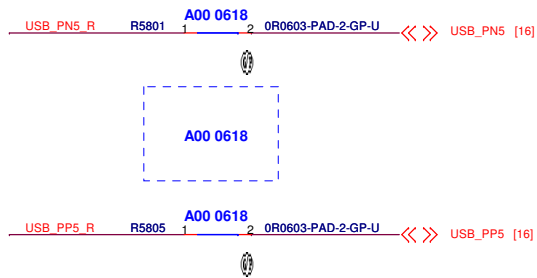
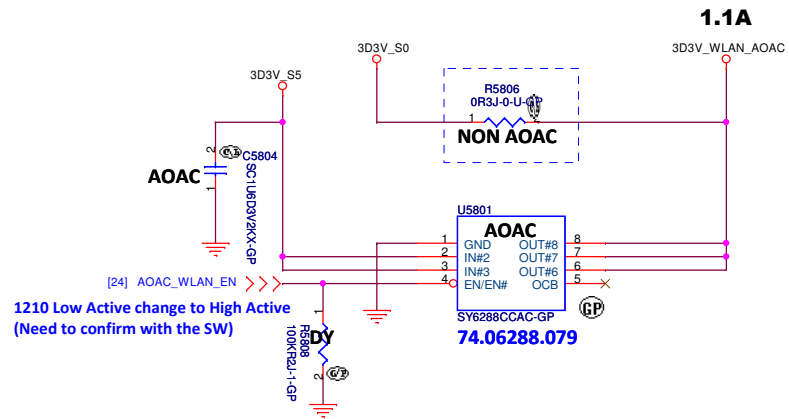
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SSID = Wireless



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Title			<b>WLAN/BT</b>	
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Title

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Size  
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Document Number  
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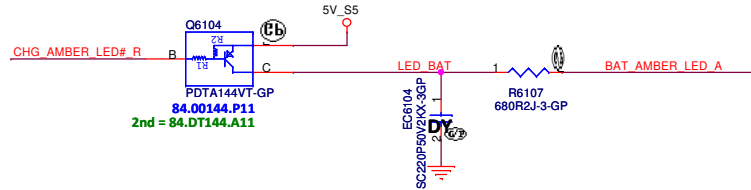
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Rev  
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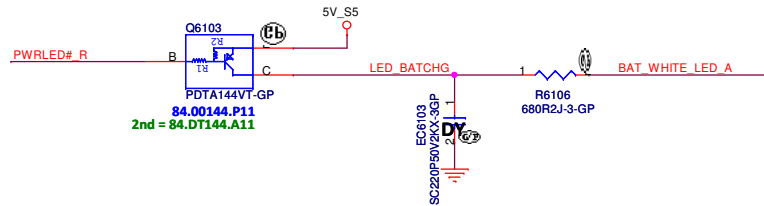
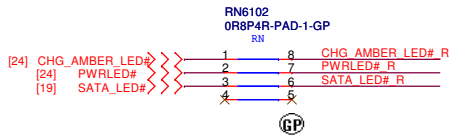
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SSID = User.Interface

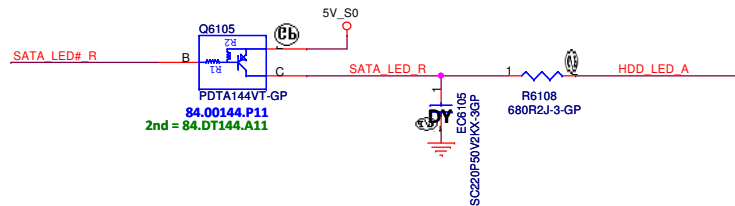
### Battery LED1(Amber\_LED) LOW acted from KBC GPIO



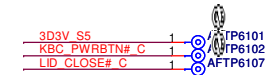
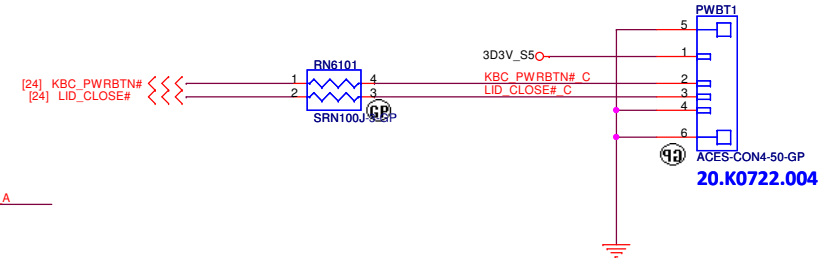
### Power & Battery LED2(White\_LED) LOW acted from KBC GPIO



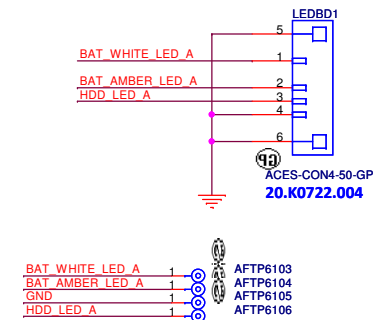
### SATA HDD LED



### PWRBTN CONN



### LED board CONN



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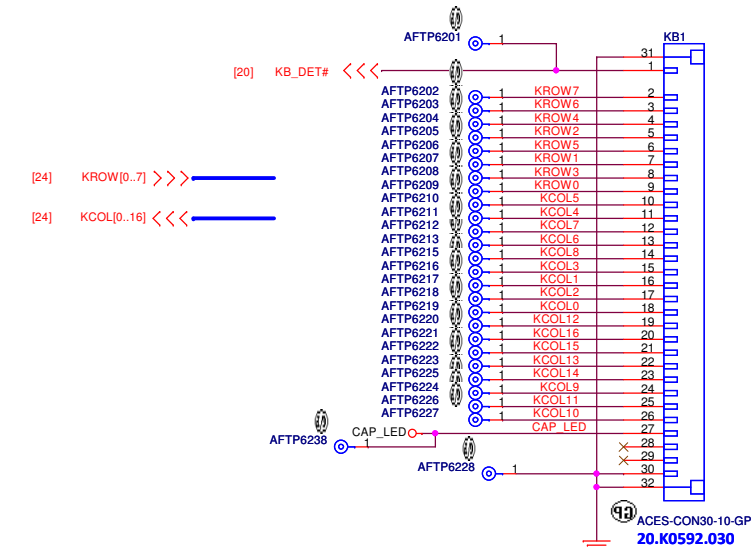


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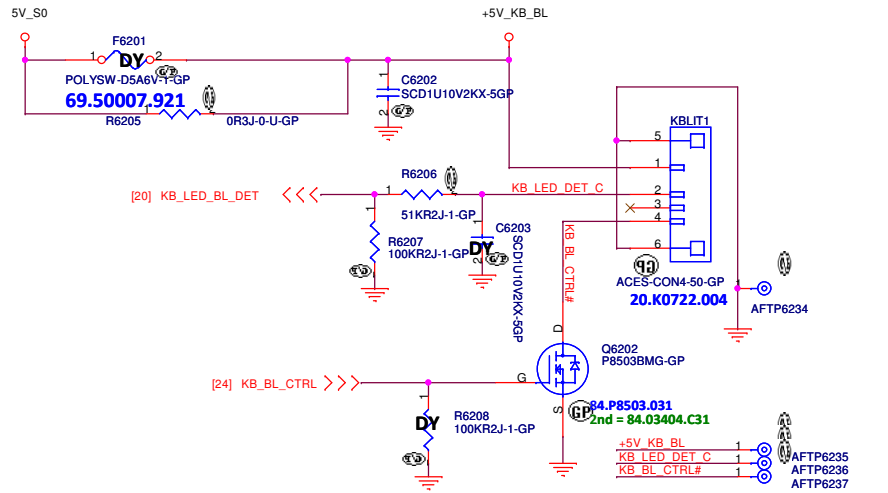
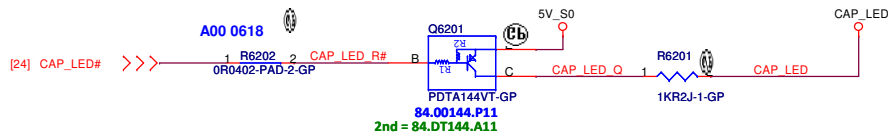
File		LED Bar/Power Button	
Size	Document Number	Rev	
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SSID = KBC

Internal Keyboard Connector

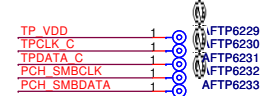
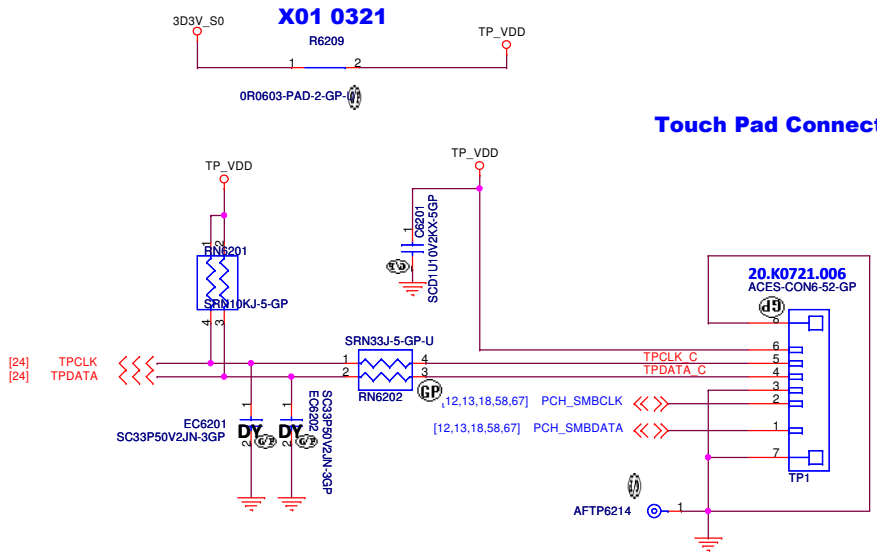


CAP LED Control  
LOW acted from KBC GPIO

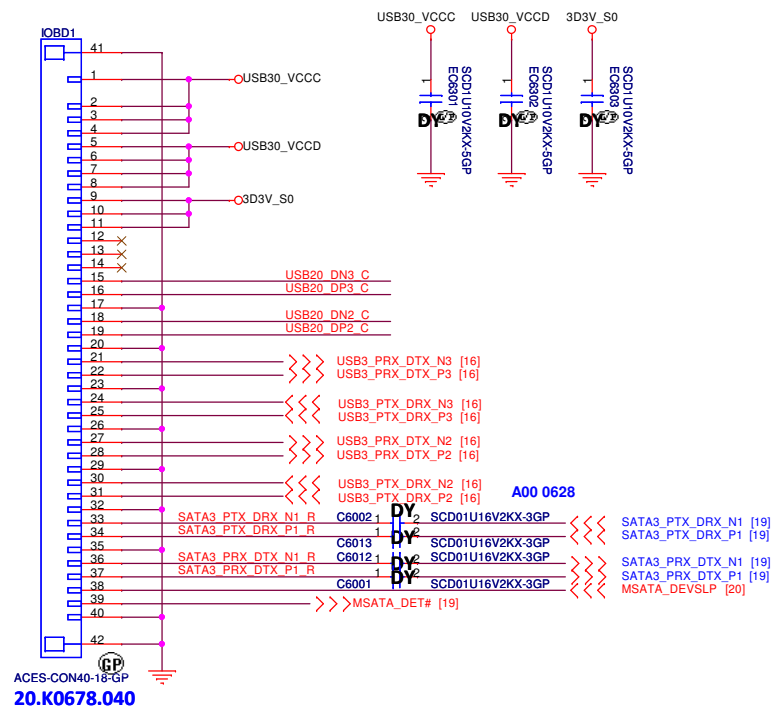


SSID = Touch.Pad

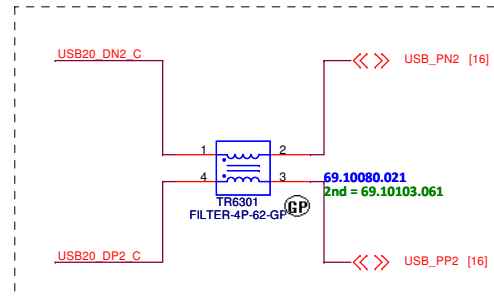
Touch Pad Connector



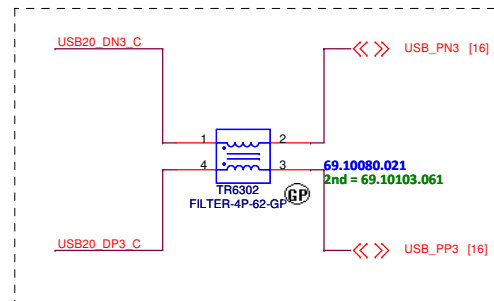
SSID = User.Interface



A00 0618



A00 0618




<Core Design>



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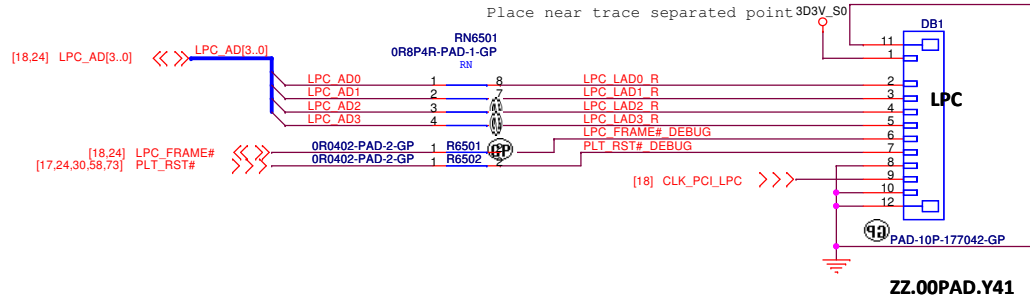
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SSID = DEBUG PORT

## Debug Connector

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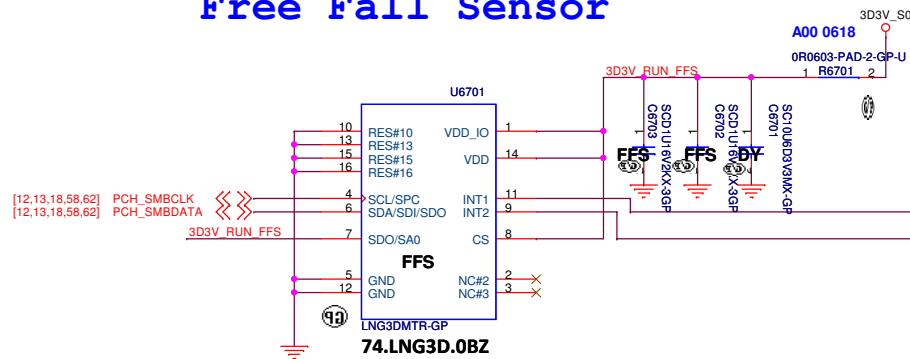
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Title <b><i>Reserved</i></b>			
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```
SSID = User.Interface
```

## Free Fall Sensor

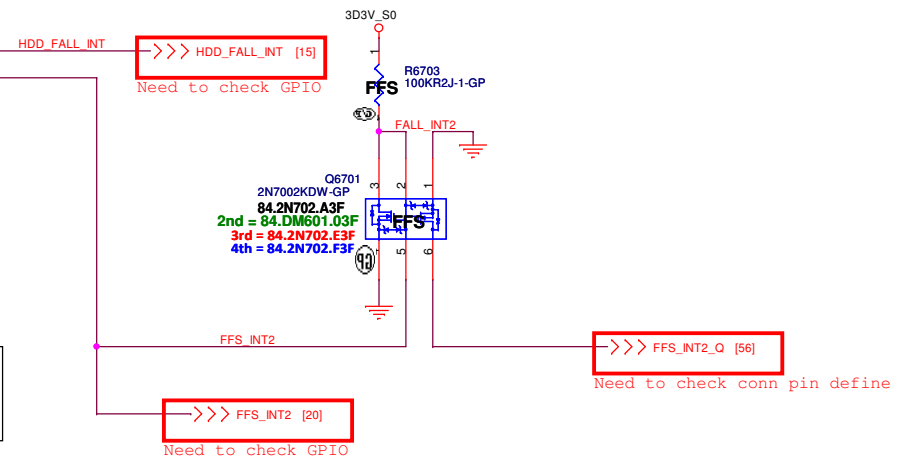


**Note:**

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

**Note:**

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



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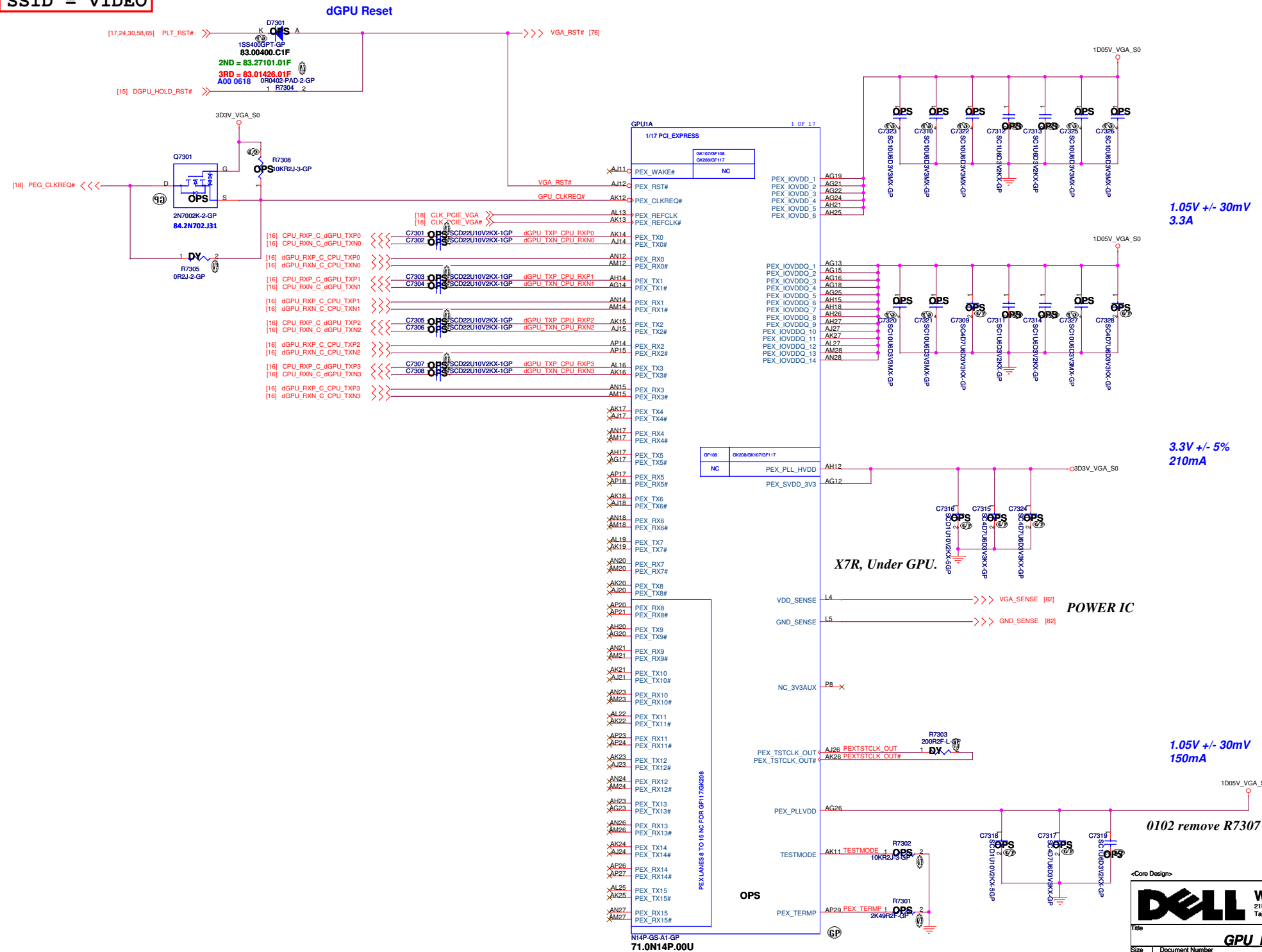
Rev

**X02**


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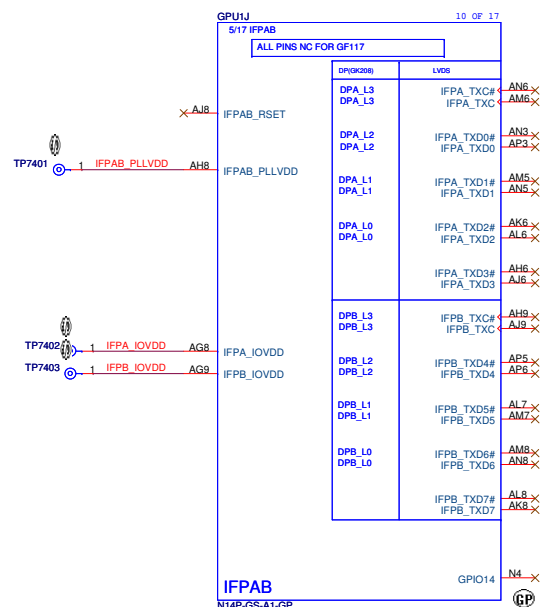
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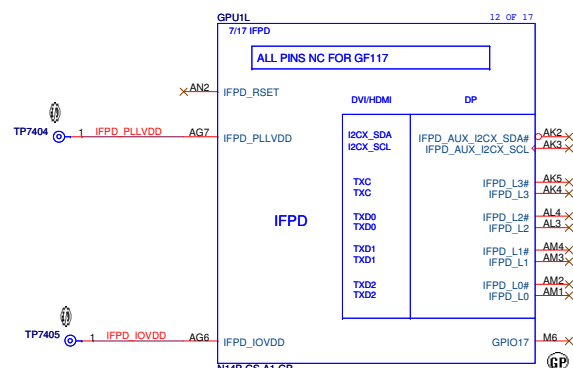
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	Title			
Size	Document Number	<b>GPU PCIE/STRAPPING(1/5)</b> <b>Hadley 15"</b>		Rev
Custom				<b>X02</b>
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SSID = VIDEO



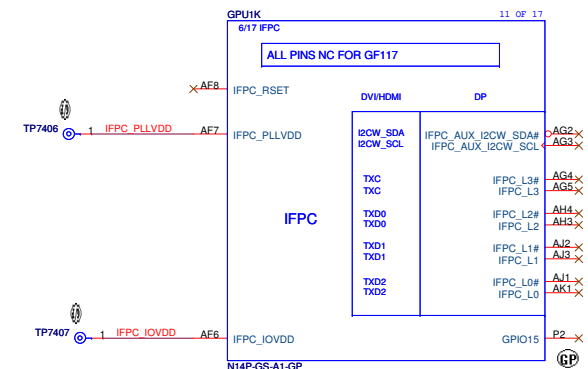
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OPS



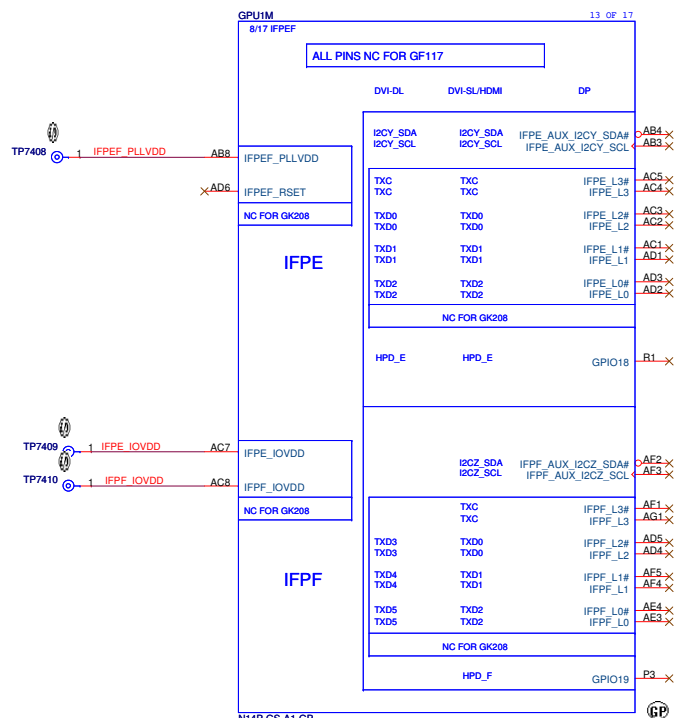
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OPS



71.0N14P.00U

OPS



71.0N14P.00U

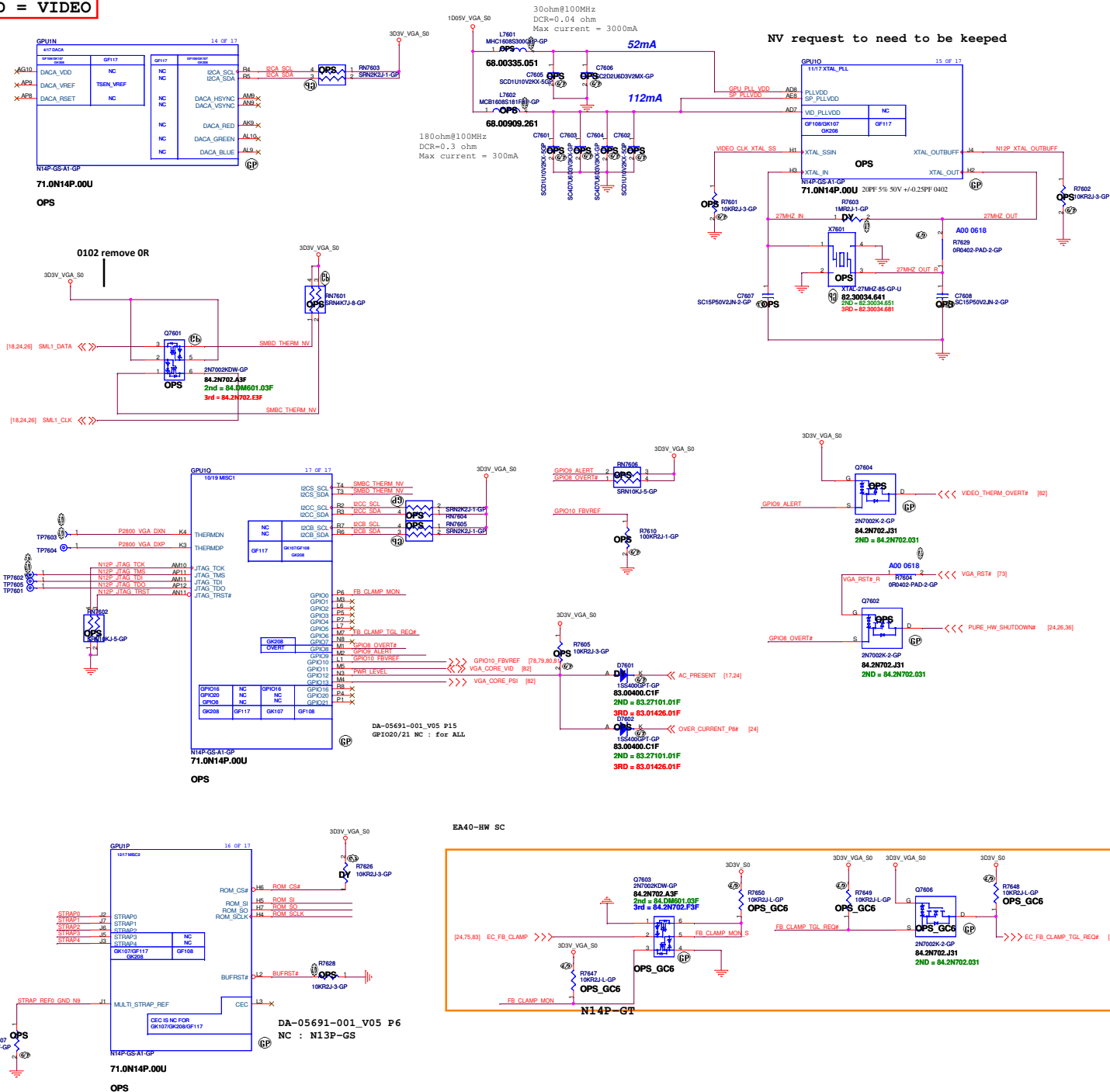
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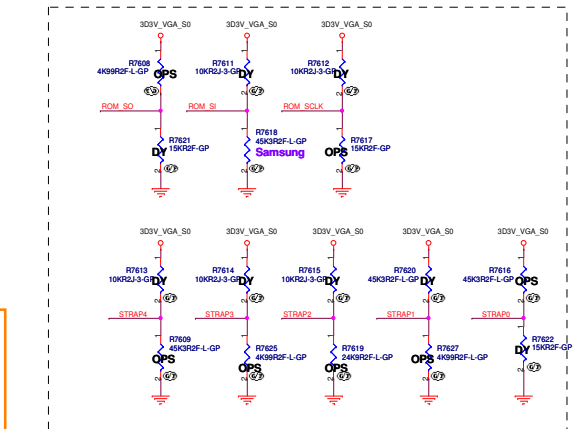


Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

GPU Product Name	N14P-GT
NV-Internal Chip Part # (used on labels of packaging bag/box materials)	GK107-750
Device ID	0x0FE4
Memory interface	GDDR5
Package	GB4-128

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x6	1.35V/ 1.35V	H5GQ2H24FR-T2C	2000	N/A	Production candidate
	Samsung	0x7	1.35V/ 1.35V	K4G20325FD-FC04	2000	1219	Post-production candidate

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCL	0	0	1	0
ROM_SI	0	1	1	1
ROM_SO	0	0	0	0
STRAP0	1	0	1	0
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	0	0	0	0
STRAP3	0	0	0	0
STRAP4	0	1	1	1

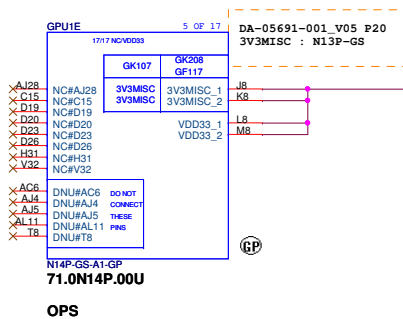
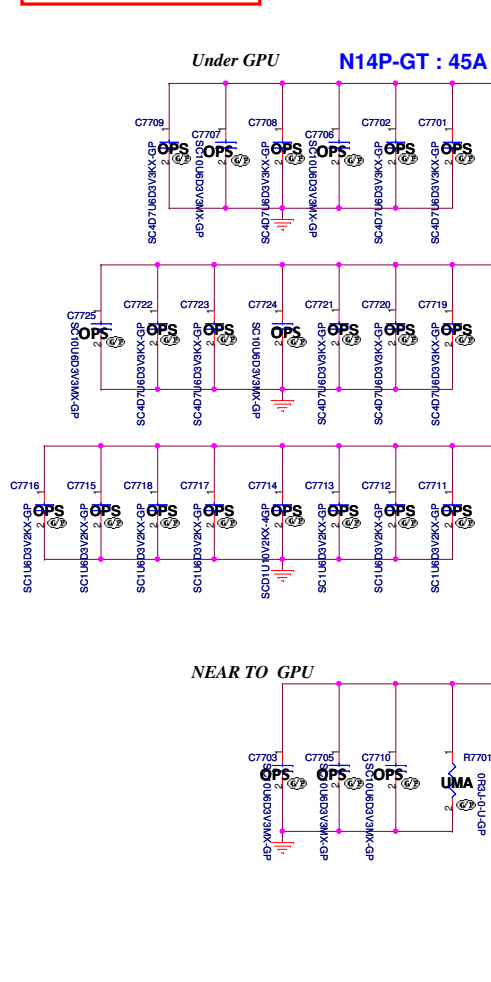


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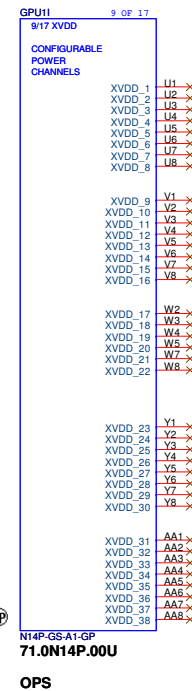
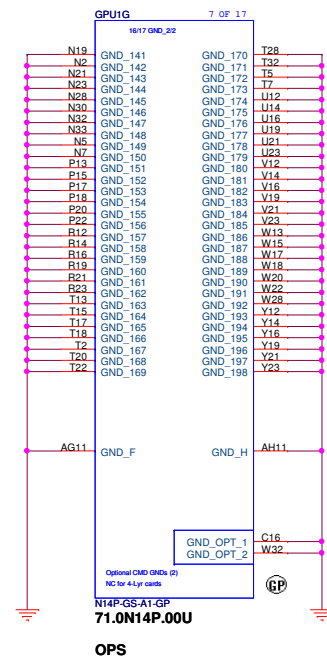
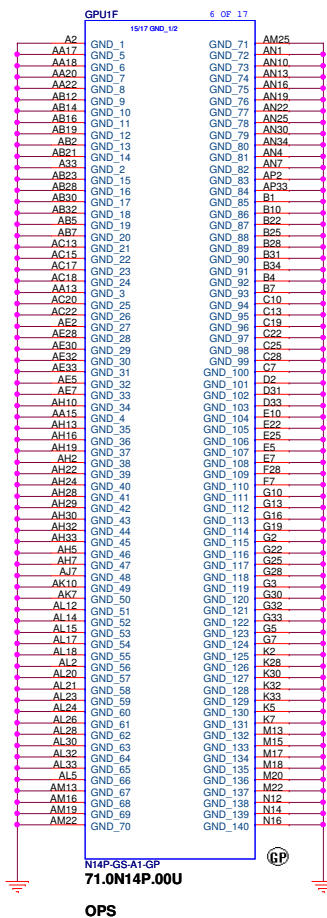
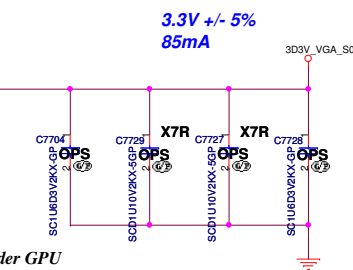
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0.1U Under GPU  
4.7U NEAR TO GPU  
1U NEAR TO GPU



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**GPU POWER(4/5)**

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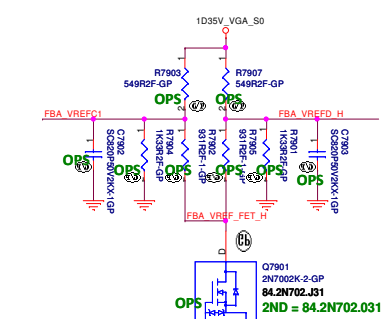
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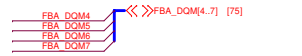
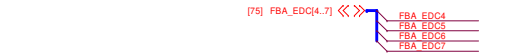
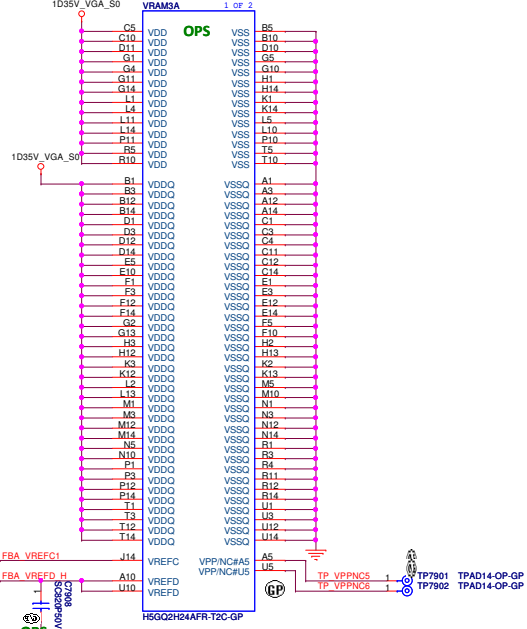
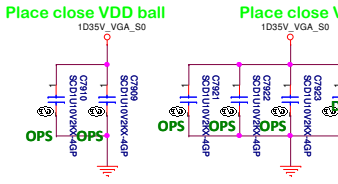
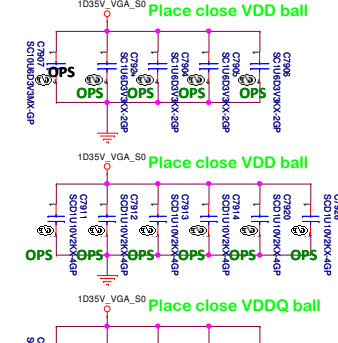
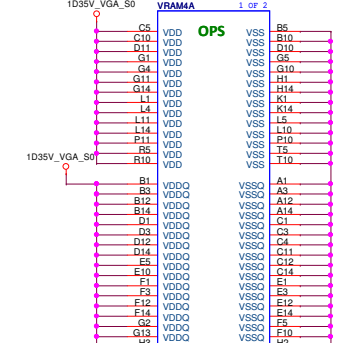
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### Frame Buffer Partition A-Upper Half

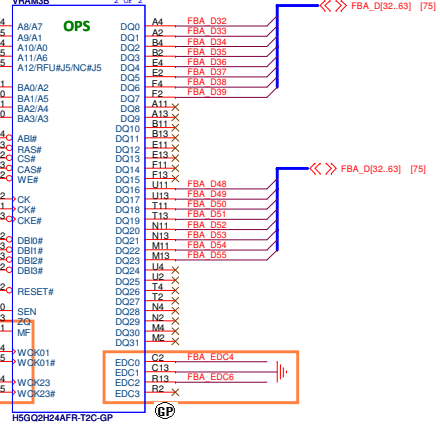


#### FBVREF Termination

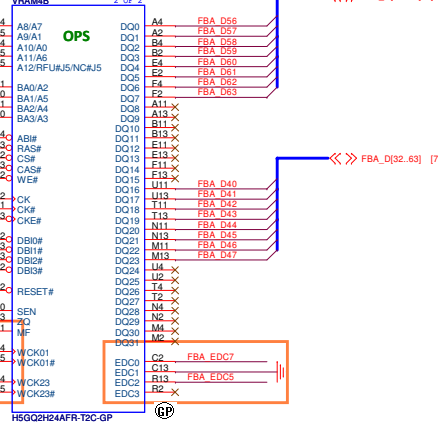
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



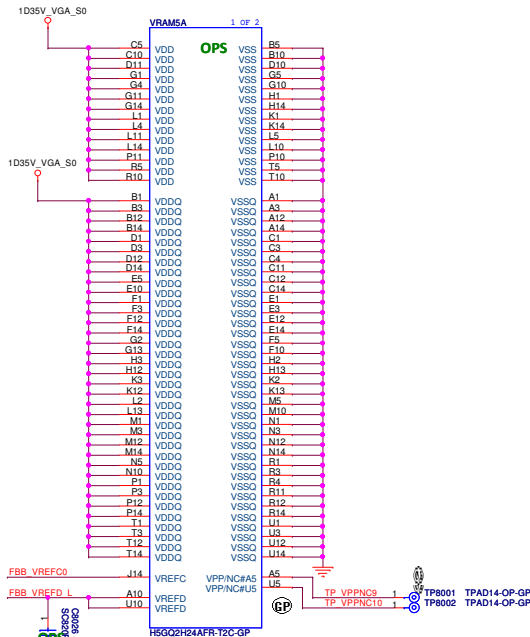
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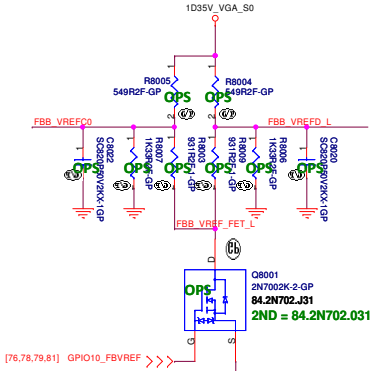
### Mirrored(MF=1)



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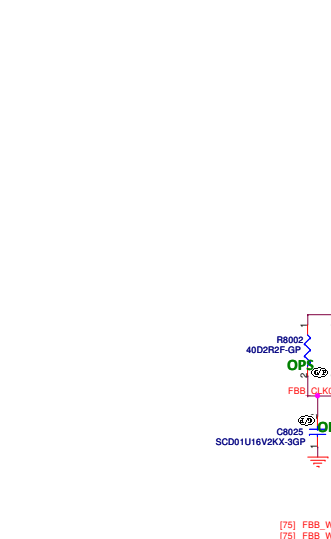
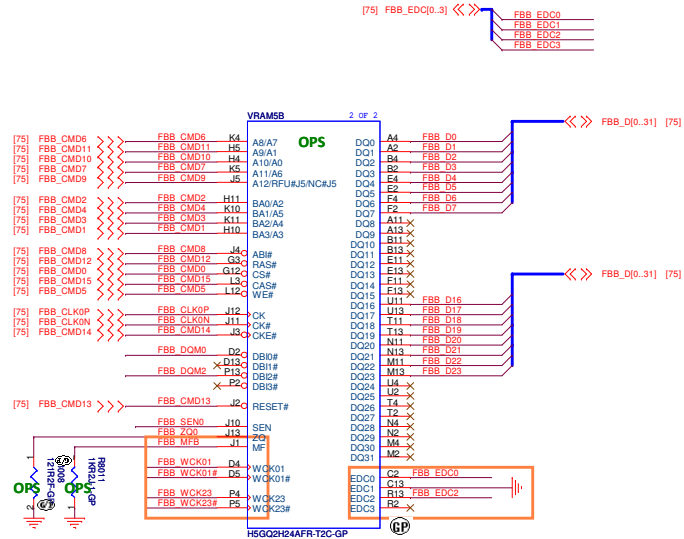
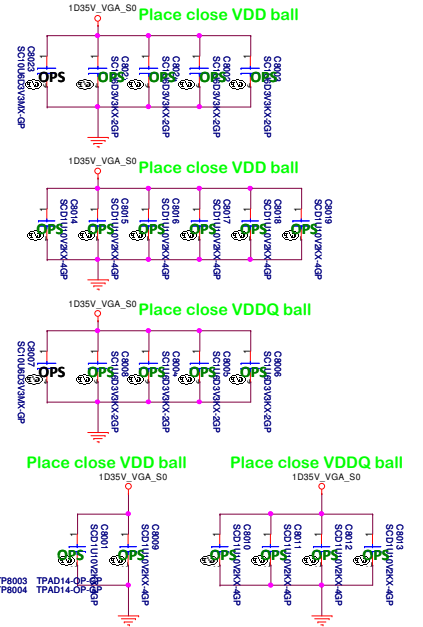
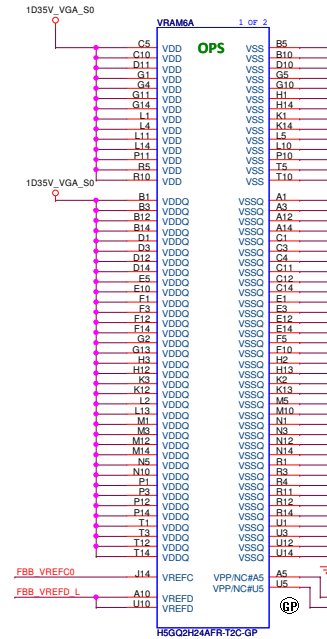


### Frame Buffer Partition B-Lower Half

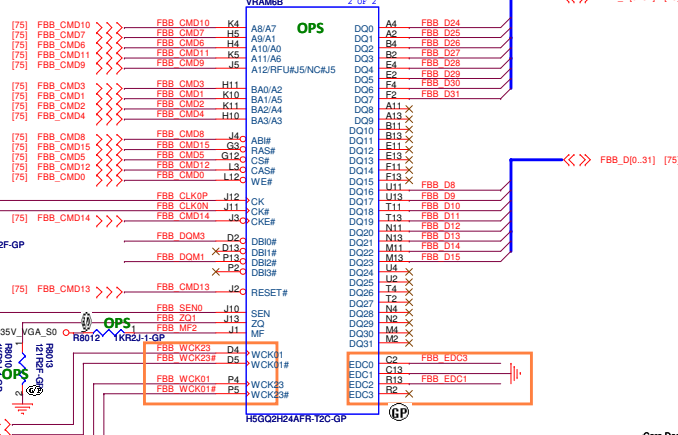


#### FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



### Mirrored (MF=1)



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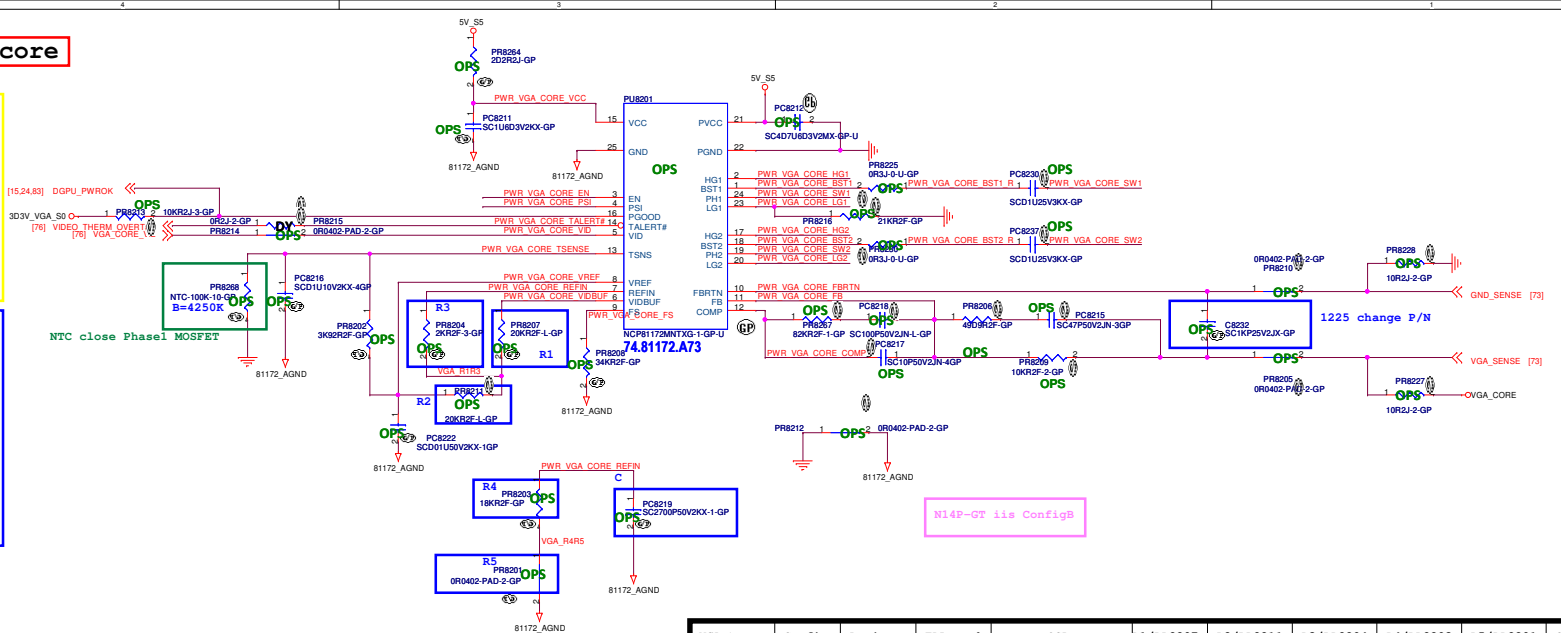
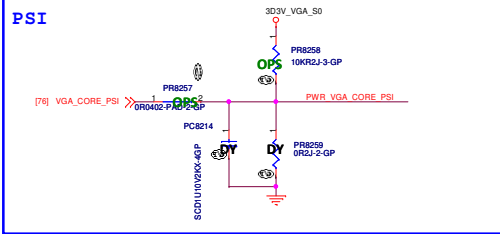
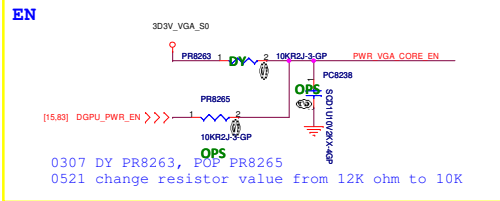
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File: **GPU-VRAM5.6 (3/4)**  
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# SSID = PWR.Plane.Regulator\_vga\_core



VGA type	Config	Design Current	EDP-peak	OCF	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8203	R5/PR8201	C/PC8219
N14P-LP	B	25A	35A	38.5A<OCF<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GE	B	27A	40A	44A<OCF<52A	20K	20K	2K	18K	0	2.7nF
N14P-GS	B	38A	60A	66A<OCF<78A	20K	20K	2K	18K	0	2.7nF
N14P-TS	B	45A	75A	82.5A<OCF<97.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV	B	24A	35A	38.5A<OCF<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV2	B	32A	55A	60.5A<OCF<71.5A	20K	20K	2K	18K	0	2.7nF
N14M-GS	B	26A	45A	49.5A<OCF<58.5A	20K	20K	2K	18K	0	2.7nF
N14M-LP	B	22A	35A	38.5A<OCF<45.5A	20K	20K	2K	18K	0	2.7nF
N14M-GL	C	24.33A	35.42A	38.96A<OCF<46.04A	39K	30K	3K	24K	3K	1.8nF
N14M-GE	C	35A	40.89A	44.98A<OCF<53.16A	39K	30K	3K	24K	3K	1.8nF
N14E-GTX	A	95A	125A	137.5A<OCF<162.5A	39K	39K	1.5K	30K	1.5K	1.5nF
N14E-GS	B	65.16A	87.87A	96.66A<OCF<114.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE-B	B	65.37A	98.6A	108.5A<OCF<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE	B	65.37A	98.6A	108.5A<OCF<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GL	B	46.35A	71.83A	79.01A<OCF<93.98A	20K	20K	2K	18K	0	2.7nF

Table 1. PWM-VID Spec and Component Values


PWM-VID Spec	Config A	Config B	Config C
Vmin	V	0.6	0.65
Vmax	V	1.2	1.15
Vboot	V	0.875	0.9
Voltage Step Vstep	mV	6.25	6.25
Number of Voltage Levels N	level	96	96
PWM Frequency F <sub>PWM</sub>	MHz	1.125	1.125
PWM Minimum Pulse Width T <sub>DMH</sub>	ns	9.26	9.26
VID Transient Time T	us	<100	<100
Component Value			
R1 (1%)	KΩ	39	39
R2 (1%)	KΩ	39	30
R3 (1%)	KΩ	1.5	2
R4 (1%)	KΩ	30	18
R5 (1%)	KΩ	1.5	0
C	nF	1.5	2.7

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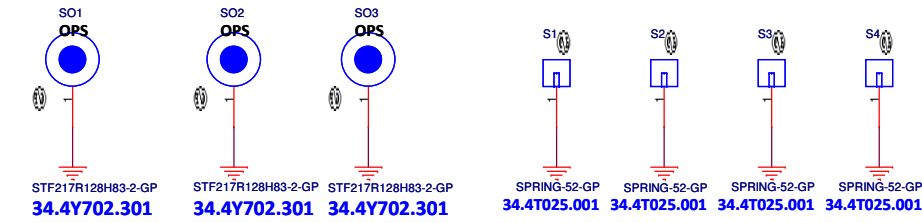
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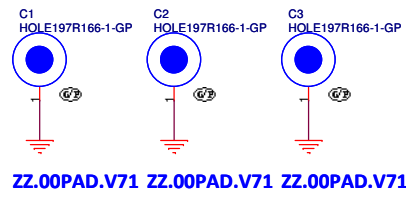
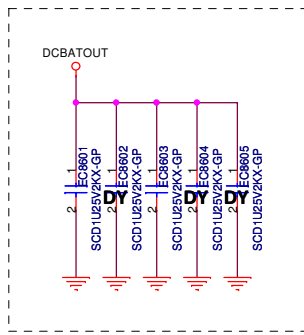
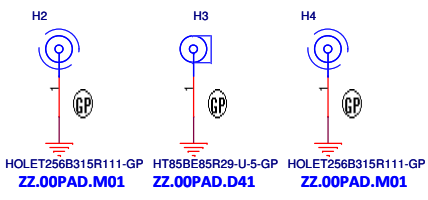
Date: Friday, June 28, 2013

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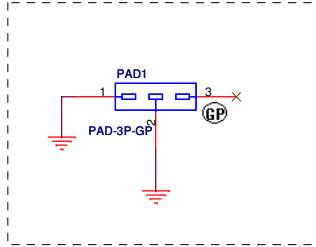
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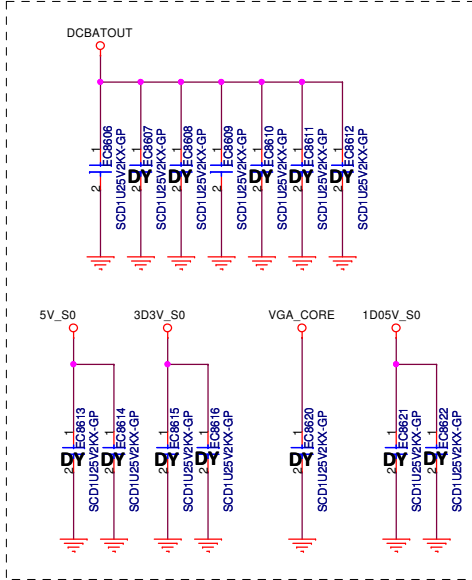
0116 Add RF CAP



0528 Add NPTH hole




0117 Add EMC CAP



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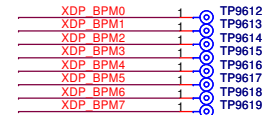
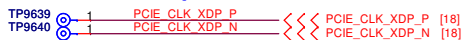
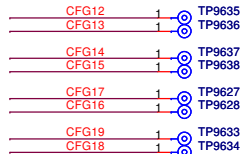
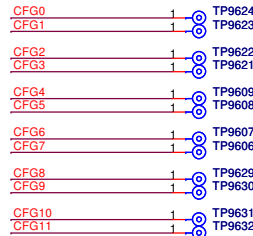
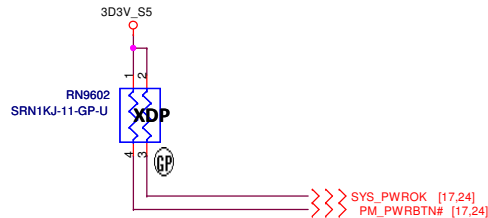
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SSID = XDP

### CPU XDP



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PCH Strapping

Name	Schematics	Notes

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION

PCIE Routing

LANE1	X
LANE2	X
LANE3	Mini Card1 (WLAN)
LANE4	X
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	
3	
4	
5	


USB Table

Pair	Device
0	USB port 1, with Power Share
1	USB 2.0 HDMI
2	USB port2 (usb redriver)
3	X
4	Touch Panel
5	Card Reader
6	BLUETOOTH
7	CAMERA

SMBus ADDRESSES

I <sup>2</sup> C / SMBus Addresses	CHIEF RIVER ORB	
	Address	Bus
Device EC SMBus 1 Battery 0 CHARGER FS8122 (HDMI Switch) (Bottom Dock) USB3.0 redriver FS8710 (Bottom Dock)	0x16 0x12 0x9E 0x40	BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 Battery 1 PCH Discrete VGA Thermal FS8321 HDMI level shifter NCT7718W	0x16 0x96 & 0x94 0x9C or 0x9E 0x96 & 0x97 0x98 or 0x99	SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
EC SMBus 3 NCT5605Y-0 NCT5605Y-1	0x30 0x32	SMB2_CLK/SMB2_DATA SMB2_CLK/SMB2_DATA SMB2_CLK/SMB2_DATA
PCH SMBus SO-DIMMA SO-DIMMB Intel LAN 82579 G-Sensor MINI WLAN INTEL LAN82579		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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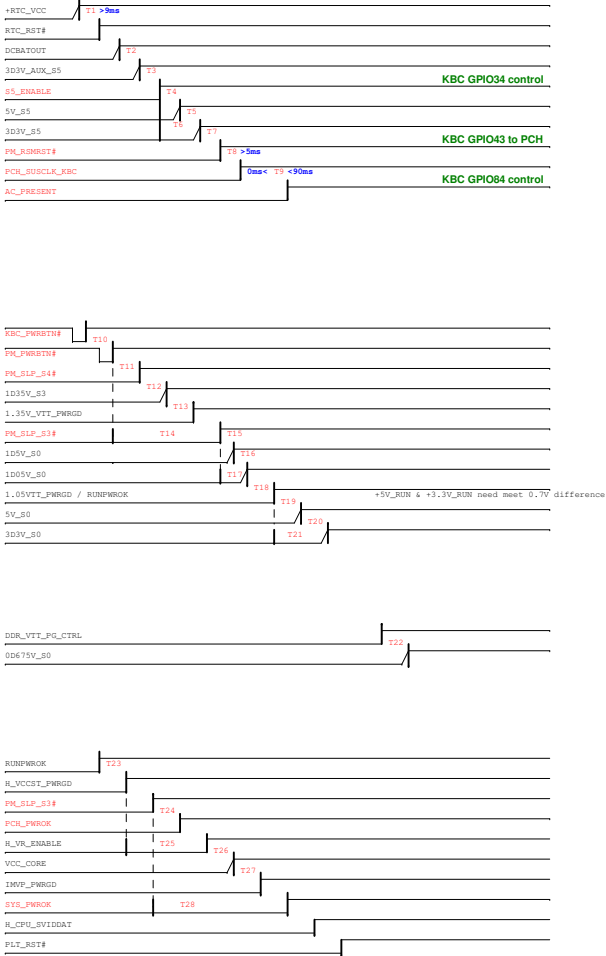
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Intel-Power Up Sequence

(AC mode)

Red printings:KBC GPIO involved



(DC mode)

Red printings:KBC GPIO involved

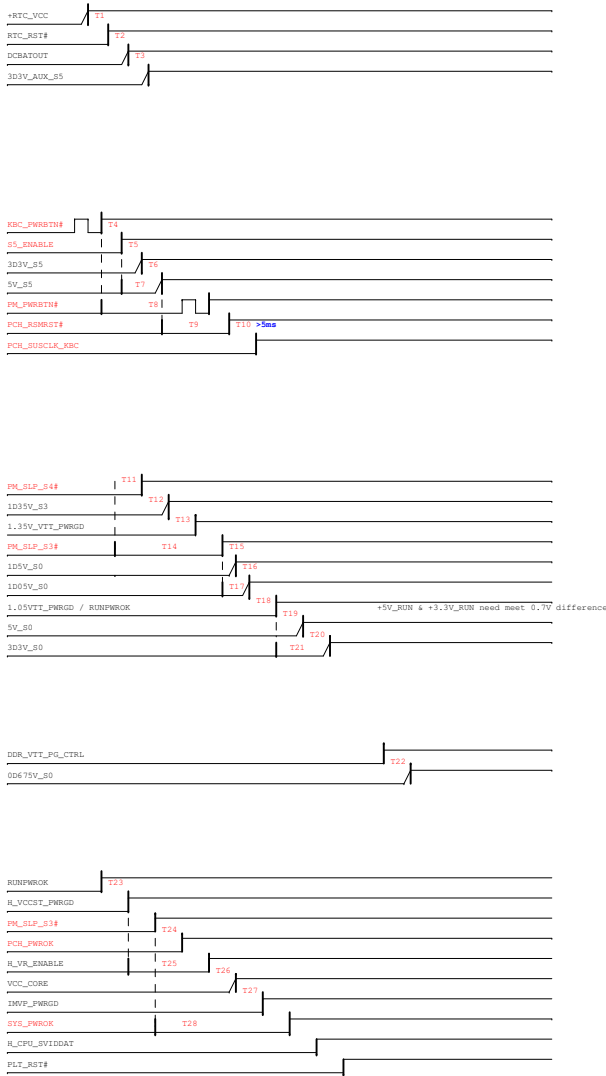
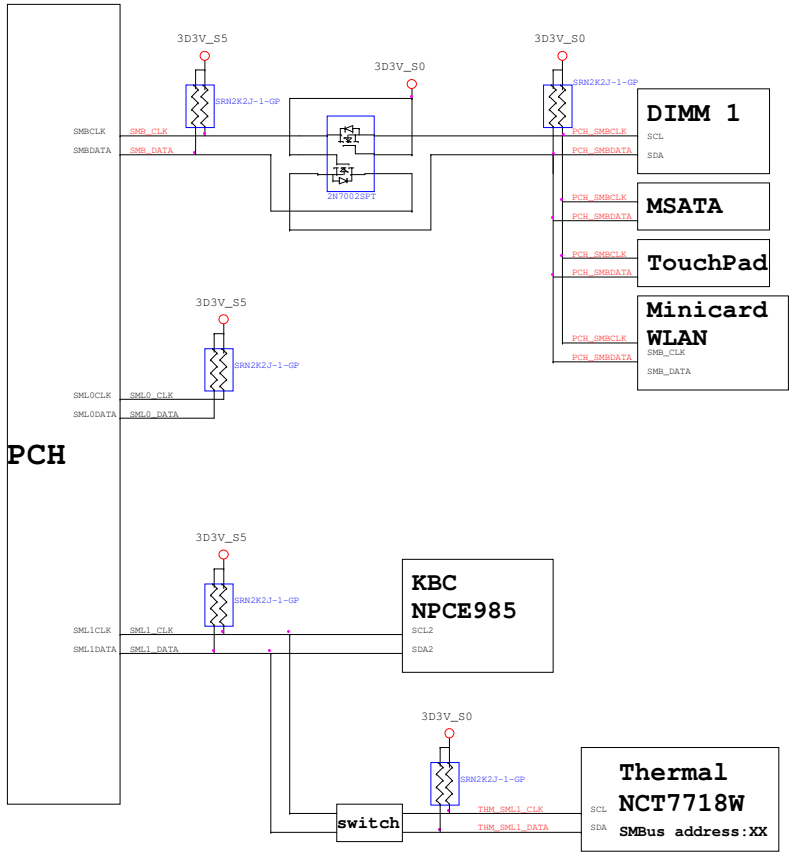


Figure 1: Haswell ULT CPU with Lynx Point PCH Power Sequencing Diagram. This diagram illustrates the power management components and their interconnections for the Haswell ULT CPU with Lynx Point PCH. The components include:

- DC/DC Converter (TPS51225CRUKR):** Provides the main system voltage (3.3V/5V) from the DC Battery or AC Adapter.
- KBC (NPCE985):** The Keyboard/Battery Controller, responsible for power sequencing and monitoring.
- TPS51367:** A DC/DC converter for the 1D05V\_S0 and 1D35V\_S3 rails.
- TPS51206:** A DC/DC converter for the 0D675V\_S0 rail.
- TPS51622:** A DC/DC converter for the VR (Voltage Regulator) rail.
- TPS51312:** A DC/DC converter for the 1D5V\_S0 rail.
- CSD97374:** A MOSFET driver for the VCC\_CORE rail.

The diagram shows the power flow from the input sources (DC Battery, AC Adapter) through the DC/DC converters and the KBC to the various output rails (3D3V\_S5, 5V\_S5, 1D05V\_S0, 1D35V\_S3, 0D675V\_S0, VR, 1D5V\_S0, VCC\_CORE). It also includes various control signals (S5\_ENABLE, SLP\_S3#, S0\_PWR\_GOOD, H\_VR\_ENABLE, H\_CPU\_SVIDDAT, IMVP\_PWRGD) and their connections to the CPU and PCH. The diagram is annotated with numbered callouts (1-12, 3a, 4a, 4b, 5) and green text notes describing the timing and assertion of various power signals.

PCH SMBus Block Diagram



KBC SMBus Block Diagram

